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Device-level co-integration of direct liquid cooling in GaN-on-SiC RF HEMTs

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Abstract Gallium nitride on silicon carbide high electron mobility transistors are key enabling devices for high power radio frequency systems. Their performance and reliability are increasingly constrained by self-heating under high power density operation. While silicon carbide substrates provide favorable thermal conductivity, continued scaling toward higher output power intensifies junction heating and exacerbates electro thermal coupling effects that degrade radio frequency performance. In parallel, stable operation at millimeter wave frequencies requires a grounding architecture with minimal parasitic inductance. Despite their interdependence, thermal management and grounding design have largely been addressed as separate challenges. Here we demonstrate a device level GaN on SiC HEMT architecture that co-integrates direct liquid cooling and low inductance grounding within a single die. An embedded microchannel is formed beneath the source region by selective etching of the GaN and SiC layers, enabling coolant flow in close proximity to the active region. In parallel, a through substrate via (TSV) establishes a shortened electrical return path through backside metallization. This co-designed electro thermal structure eliminates additional thermal interfaces while simultaneously reducing junction thermal resistance and grounding parasitics. The integrated cooling channel enables a maximum removable heat flux of 14.41 $kW \cdot cm^{-2}$ representing a 74.4 % increase compared with a reference conduction cooled package. The junction to coolant thermal resistance is reduced to 0.0061 $cm^2 \cdot K \cdot W^{-1}$, confirming the effectiveness of device level direct cooling. These thermal improvements translate directly into enhanced electrical performance, including suppressed self-heating induced resistance increase and higher drain current under identical bias conditions. This work establishes device level electro thermal co-integration as an effective design paradigm for high power density GaN radio frequency electronics, providing a scalable pathway toward simultaneous thermal reliability and electrical performance enhancement in next generation millimeter wave systems.

1. Introduction

Gallium nitride on silicon carbide high electron mobility transistors (GaN-on-SiC HEMTs) have become indispensable active devices for high power radio frequency systems, including radar, satellite communications, and fifth generation wireless infrastructure, owing to their wide bandgap properties, high breakdown field, and superior high frequency performance [1–4]. The use of a SiC substrate provides an intrinsically favorable thermal conduction pathway that supports operation at elevated power densities. Nevertheless, continued device scaling and the persistent demand for higher output power significantly intensify heat generation within the active region. The resulting self-heating elevates the junction temperature and directly degrades electrical performance through reductions in drain current and transconductance, ultimately constraining device stability and operational lifetime [5–9]. Experimental and reliability studies consistently report accelerated degradation as the junction temperature approaches approximately 150–200 °C, where thermally activated failure mechanisms such as trap accumulation, metal semiconductor interfacial reactions, and gate structure degradation become increasingly

dominant [5–7, 10]. These effects deteriorate output characteristics and substantially shorten device lifetime, establishing thermal management as a central challenge for high power GaN RF electronics.

Conventional air cooled heat sinks are increasingly inadequate for dissipating the extreme heat fluxes generated in modern RF HEMTs [11, 12]. To overcome this limitation, liquid cooling approaches based on indirect architectures, including cold plates and heat sinks, have been actively explored [13, 14]. However, the presence of multiple thermal interfaces and intervening materials introduces substantial thermal resistance, which fundamentally limits further reductions in junction temperature [15]. These constraints have driven growing interest in embedded cooling strategies, in which microchannels are formed within the device substrate to allow coolant flow in close proximity to the heat generating region. By shortening the thermal conduction path and eliminating thermal interface materials, direct cooling enables a substantial reduction in overall thermal resistance [16-18]. Representative studies have demonstrated the thermal capability of direct cooling using various architectures. Van Erp et al. reported heat flux removal on the order of 1700 $W \cdot cm^{-2}$ using embedded manifold microchannels in power electronic devices [19]. Ditri et al. integrated jet based microfluidic cooling into GaN RF monolithic microwave integrated circuits, reducing device temperature from 250 °C to 127 °C and enabling both higher output power and gain improvement exceeding 4 dB [20]. Ye et al. embedded microchannels in GaN-on-SiC devices and achieved heat removal of 2.29 $kW \cdot cm^{-2}$ together with a 19.5 % recovery in saturation current [21]. Nela et al. demonstrated direct microchannel cooling in GaN-on-Si power devices, removing 220 $W \cdot cm^{-2}$ under a 60 °C temperature rise [22]. Kang et al. simulated direct cooling using embedded manifold microchannels for GaN-on-SiC device, maintaining a temperature difference of 28.3 °C with approximately 90 mW of pump power and demonstrating fabrication feasibility through device and channel realization [23]. Although these studies clearly establish the thermal potential of direct cooling, most evaluations were performed using thin film heaters or under direct current conditions, and its implementation in practical RF devices remains largely unexplored.

In high power RF systems, thermal and electrical behaviors are inherently coupled. Localized hot spots, temperature nonuniformity, and parasitic inductance critically influence output characteristics and operational stability, particularly at millimeter wave frequencies. While direct cooling effectively reduces thermal resistance, it does not by itself address electrical parasitics that limit RF performance. Among these parasitics, source inductance associated with the grounding path plays a decisive role in high frequency operation. TSV based grounding structures have therefore been proposed as an effective approach for reducing source inductance. Several studies have explored the co-integration of TSVs and microchannels using interposer level or packaging level architectures [24, 25]. Although these approaches demonstrate the feasibility of combining thermal and electrical functionalities, they are constrained by architectural complexity and the introduction of additional thermal interfaces that diminish cooling effectiveness. As a result, direct cooling and low inductance grounding have remained fundamentally decoupled at the device level, and the combined electro thermal impact of these two strategies within a single GaN HEMT has not yet been experimentally established.

In this work, we address this limitation by demonstrating a device level GaN-on-SiC HEMT architecture that integrates an embedded microchannel for direct liquid cooling with a TSV based low inductance grounding path within a single die. The GaN and SiC layers beneath the source pad are selectively etched to form an internal cooling channel that enables coolant flow in close proximity to the active region, while a TSV provides a shortened electrical return path through backside metallization. This co-integrated structure eliminates additional thermal interfaces and simultaneously reduces junction thermal resistance and grounding parasitics. Using this architecture, we experimentally investigate the coupled thermal and electrical behavior under realistic operating conditions, revealing substantial reductions in junction temperature and thermal resistance together with measurable improvements in electrical output characteristics. These results establish device level co-design of thermal and electrical pathways as an effective strategy for next generation high power GaN RF devices.

2. Method

Device fabrication and packaging, thermal modeling, and integrated electro thermal characterization were employed to evaluate the coupled thermal and electrical behavior of a GaN-on-SiC HEMT incorporating a TSV defined embedded cooling channel. These approaches enable quantitative assessment of device level electro thermal interactions under realistic operating and cooling conditions.

2.1 Device-level thermal modeling

A three dimensional steady state heat conduction model was developed to predict the junction temperature distribution of the GaN-on-SiC device under various electrical power dissipation and cooling conditions. The computational domain used in the analysis is shown in Fig. 1. Fig. 1(a) presents the overall simulation domain corresponding to the fabricated device. The total die size is 4.5 × 2.7 mm. The backside cooling channel was modeled, having a width (W_{ch}) of 80 μm, a height (H_{ch}) of 100 μm, and an axial length (L_{ch}) of 1000 μm. To reduce computational cost while preserving thermal symmetry, a quarter symmetry model was applied with respect to the device center, resulting in a simulated domain of 2.25 × 1.35 mm. Fig. 1(b) shows an enlarged cross sectional view of the device region where symmetry boundary conditions were imposed. The simulation domain includes a GaN layer with a thickness of 2 μm and an underlying SiC substrate with a thickness of 100 μm. An AlN interlayer with a thickness of 17.5 nm was incorporated between the GaN layer and the SiC substrate to account for the thermal

boundary resistance at the heterointerface. The width and length of a single gate finger are 100 μm and 1 μm respectively, and the device consists of 48 gate fingers, consistent with the fabricated structure. The gate fingers are arranged in repeating groups of six. Uniform heat flux was applied to each gate finger to represent the spatial distribution of power dissipation associated with the expanded source pad structure.

Three heat flux conditions of 5 $kW \cdot cm^{-2}$, 10 $kW \cdot cm^{-2}$, and 15 $kW \cdot cm^{-2}$ were applied based on the defined active area. These heat flux values were converted and imposed according to the effective gate finger area in the numerical model. Convective heat transfer boundary conditions were applied at the bottom surface of the device to represent cooling by the embedded microchannel, with the ambient temperature set to 20 °C, while all remaining external surfaces were treated as adiabatic boundaries. The material properties used in the numerical analysis are summarized in Table 1 and include the density, specific heat capacity, and thermal conductivity of GaN, AlN, Au, and SiC. For AlN, the thermal conductivity was derived from a reported thermal boundary resistance value of 3.3×10^{-8} $m^2 \cdot K \cdot W^{-1}$ [26]. For SiC, temperature dependent thermal conductivity was considered, with values ranging from 222 $W \cdot m^{-1} \cdot K^{-1}$ to 343 $W \cdot m^{-1} \cdot K^{-1}$ over the temperature range relevant to this study.

Table 1. Material properties used in the thermal modeling of the GaN-on-SiC device.

Material	ρ ($kg \cdot m^{-3}$)	C_p ($J \cdot kg^{-1} \cdot K^{-1}$)	K ($W \cdot m^{-1} \cdot K^{-1}$)
GaN	6150	490	139
AlN	3260	740	0.5
Au	19320	129.8	297
SiC	3210	$-3.0 \times 10^{-10}x^4$ $+2.0 \times 10^{-6}x^3$ $-3.4 \times 10^{-3}x^2$ $+3.2089x$ $+2.4299$	$2.0 \times 10^{-10}x^4$ $-9.0 \times 10^{-7}x^3$ $+1.9 \times 10^{-3}x^2$ $-1.7393x$ $+716.89$

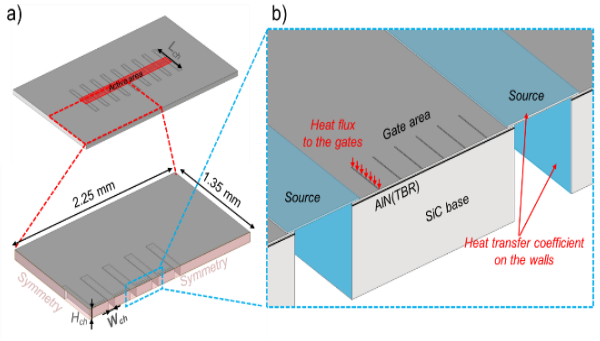

Fig. 1. Computational domain and boundary conditions for thermal analysis: (a) three-dimensional computational domain of the GaN HEMT device; (b) cross-sectional view of the device structure and boundary conditions. The figure illustrates the quarter-symmetry numerical model, including the GaN, AlN, and SiC layers, the application of uniform heat flux at the gate regions, convective boundary conditions at the backside and source-pad sidewalls, and adiabatic conditions on the remaining external surfaces.

2.2 Device and package fabrication and integration

2.2.1 Device-level fabrication of the GaN-on-SiC HEMT structure

Fig. 2 illustrates the fabrication process flow of the GaN-on-SiC HEMT incorporating an embedded cooling channel and TSV based grounding. The devices were fabricated on a commercial 4-inch AlGaN GaN on SiC epitaxial wafer obtained from Wolfspeed Inc. Front side processing was first performed to define the active device structure and electrical contacts. A Ti/Al/Ni/Au metal stack was deposited and annealed at 780 °C for 40 s under an N_2 atmosphere to form ohmic contacts to the two dimensional electron gas layer. Device isolation was achieved by ion implantation to electrically separate adjacent devices. A SiN passivation layer was subsequently deposited by plasma enhanced chemical vapor deposition (PECVD) to protect the device surface and prevent electrical shorts between metal interconnects. A Ti/Au metallization layer with a thickness of 30/500 nm was then deposited as the first interconnect layer. Gate patterning was carried out by electron beam lithography followed by deposition of a Ni/Au Schottky gate metal with a thickness of 60/400 nm. An Au air bridge was formed by electroplating to electrically connect the source pads, completing the front side device fabrication.

Back side processing was performed to realize the embedded cooling channel and TSV based grounding structure. The device wafer was temporarily bonded to a carrier wafer using a polymer based adhesive (PMMI), prior to substrate thinning to approximately 100 μm. A Ti/Au base metal layer with a thickness of 3/8 nm was deposited on the thinned backside surface. A backside channel pattern was defined using AZ 4620 photoresist, and a Ni hard mask was subsequently formed by electroplating. Using the Ni hard mask, the SiC substrate was etched by SF_6 based inductively coupled plasma (ICP) etching to form microchannels with dimensions of W_{ch} = 80 μm and L_{ch} = 900 μm while simultaneously exposing the bottom surface of the source pads. After etching, the Ni hard mask was removed using an

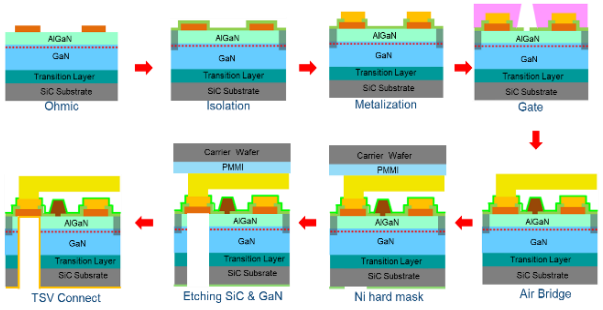

Fig. 2. Device fabrication process flow. The GaN HEMT device was fabricated on a commercial 4-inch AlGaN/GaN-on-SiC epitaxial wafer. The process con-sists of front-side device fabrication, including ohmic and Schottky con-tact formation, device isolation, and surface passivation, followed by backside wafer thinning and microchannel etching into the SiC substrate beneath the source pad. TSV were subsequently formed to electrically connect the front-side source pad to the backside metallization.

HNO_3 solution, followed by removal of residual Au using a dedicated Au etchant. The remaining Ti layer was removed using buffered oxide etchant (BOE), and surface residues were eliminated by HCl sonication. Following microchannel formation, the GaN layer was selectively etched using Cl_2 based ICP etching to complete the channel opening beneath the source pad. A Ti/Au metallization layer with a thickness of 50/300 nm was deposited by sputtering to metalize the via sidewalls and exposed backside source pads, thereby forming TSV that electrically connect the front side source pads to the backside metallization. For subsequent die bonding and package integration, Au with a thickness of 2700 nm was electroplated on the backside surface, followed by deposition of a Sn/Au layer with a thickness of 1900/20 nm by electron beam evaporation.

Fig. 3 presents optical and cross sectional images of the fabricated GaN-on-SiC HEMT. The device has a die size of 4.5 × 2.7 mm^2 and a total gate width of 4.8 mm implemented using a multi-finger architecture to support high power operation. In the proposed structure, the region beneath the source pads is selectively etched and utilized as a coolant flow channel, which necessitates local expansion of the source pad width to ensure smooth coolant transport. Uniform expansion of all source pads would significantly increase the overall device area and degrade RF performance. To avoid this trade off, a periodically widened gate pitch structure was adopted to selectively expand the source pads beneath the device while maintaining compact interconnect routing. Gate and drain interconnects were placed in the upper and lower regions between the expanded source pads and arranged in a tree type configuration to minimize RF performance degradation. The device consists of eight gate finger groups, which reduces interconnect length while ensuring uniform signal distribution. Fig. 3(b) shows an enlarged view of the source gate drain region between the expanded source pads. Channel current flowing between the drain and source is modulated by the gate voltage following conventional HEMT operation. Fig. 3(c) shows a cross sectional image of the fabricated structure, confirming that the GaN and SiC layers beneath the source pad were etched to form an embedded coolant flow channel while simultaneously providing electrical connection between the front side and backside metallization. These results confirm that the embedded cooling channel and TSV based grounding path are integrated within a single GaN-on-SiC HEMT die.

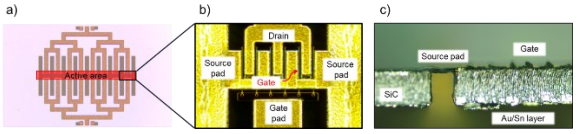

Fig. 3. Optical and cross-sectional images of the fabricated GaN HEMT device: (a) top-view optical image of the device; (b) magnified view of the multi-finger gate structure and widened source pads; (c) cross-sectional view of the device structure. The figure presents the fabricated GaN HEMT, highlighting the multi-finger gate architecture, the periodically widened source pads for embedded cooling, and the etched GaN/SiC layers with backside Au/Sn metallization enabling electrical connection between the front and backside of the device.

To enable comparative evaluation of thermal performance, a reference device without an embedded cooling channel was fabricated alongside the integrated device. The reference GaN-on-SiC device was fabricated from the same wafer as the device used in this study and thinned to a substrate thickness of 200 μm. It has a die size of 2.3 × 1.0 mm^2 and employs a multi-finger configuration consisting of 40 gate fingers with a total gate width of 4.8 mm. This device was used as a control sample to isolate the effect of the embedded cooling channel and TSV based integration on junction temperature behavior.

2.2.2 Package assembly and electrical

A dedicated package was designed and fabricated to enable simultaneous electrical operation and direct liquid cooling of the GaN-on-SiC HEMT. The package architecture was developed to support controlled electro thermal performance evaluation under realistic operating conditions. Fig. 4(a) schematically illustrates the structure of the fabricated package. The device incorporating the embedded cooling channel was bonded to an Al submount containing a machined manifold structure using an electrically conductive epoxy. This configuration provides both mechanical fixation and electrical grounding of the source electrode through the TSVs integrated within the device. To ensure reliable operation under liquid cooling conditions, the bonding interface between the device and the Al submount was additionally sealed to prevent coolant leakage during operation. Following die attachment, the package housing was fabricated by three dimensional printing and bonded to the Al submount to complete the package assembly. The housing was designed to incorporate inlet and outlet ports for coolant delivery as well as ports for temperature and pressure measurements. This design enables quantitative characterization of the coupled thermal and fluidic behavior of the device under controlled coolant flow conditions.

Fig. 4(b) shows an optical image of the assembled package in which the electrical interconnections and the cooling structure are fully implemented. An Au plated printed circuit board (PCB) was used as the electrical interface for gate and drain biasing. The gate and drain electrodes of the device were connected to the PCB by wire bonding, allowing stable electrical connection

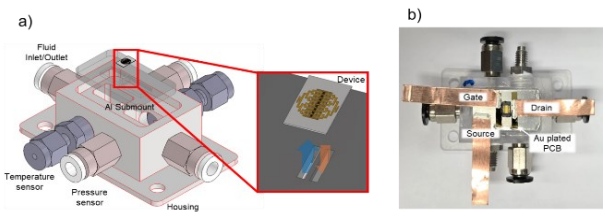

Fig. 4. Power and thermal co-measurement package with embedded cooling: (a) schematic illustration of the fabricated package architecture; (b) photograph of the assembled power and thermal co-measurement package. The device is bonded to an Al submount with an integrated coolant manifold, electrically interfaced via an Au-plated PCB, and grounded through TSVs, enabling coupled thermal and electrical measurements.

to external power supplies. Electrical grounding was achieved by connecting the Al submount to an external ground through Cu tape and conductive Ag paste. This configuration ensures a low resistance and low inductance grounding path that complements the TSV based grounding structure within the device.

For benchmarking thermal performance, a reference device was packaged using a conventional copper molybdenum copper (CMC) package (PKG 14041, Inc Kostecsys). The reference device was mounted on a metal jig package commonly used for RF amplifier characterization, in which heat dissipation occurs predominantly through thermal conduction. This reference configuration was used to provide a baseline for comparison with the directly cooled package and to isolate the thermal performance gains enabled by the embedded cooling channel and TSV based integration.

2.3 Integrated electro-thermal characterization

2.3.1 Experimental setup and measurement procedure

A closed loop thermal fluid flow system was constructed to evaluate the electro thermal performance of the GaN-on-SiC HEMT under direct liquid cooling conditions. Fig. 5 shows the experimental setup used for the measurements. The system was designed to independently control the electrical power dissipated in the device while simultaneously monitoring the resulting thermal and fluidic responses under steady coolant flow. Device heating was achieved by applying DC power across the drain source terminals using a power supply (HP 6030 A, Hewlett Packard). The input power was increased in increments of 5 W, with the total dissipated power maintained below 35 W depending on the coolant flow rate to ensure safe operation of the measurement system. The applied drain source voltage was monitored using a resistive voltage divider composed of 49 kΩ and 1 kΩ resistors. The drain source current was measured by sensing the voltage drop across a 0.01 Ω shunt resistor connected in series with the device. The dissipated electrical power was determined from the measured drain source voltage and current and was used solely to generate heat within the device.

Coolant was supplied to the embedded microchannel through a closed loop circulation system driven by a micropump (DEMSE X21, Micropump). The volumetric flow rate was measured using a Coriolis mass flow meter (mini CORI-FLOW M14, Bronkhorst). The inlet and outlet pressures of the microchannel were monitored using a differential pressure sensor and an absolute pressure sensor (PXM-409 and PX191, Omega Engineering). Coolant temperatures at the inlet and outlet were measured using calibrated K-type thermocouples (KMQSS-062, Omega Engineering). The junction temperature of the device was measured using a non-contact infrared camera (A6753sc, FLIR Systems). Prior to the measurements, the surface emissivity of the GaN layer was calibrated to a value of 0.57 to ensure accurate temperature extraction. Electrical, thermal, and fluidic signals were continuously acquired using data acquisition moules (NI-9220 and NI-9217, National Instruments) and recorded for post processing using a custom LabVIEW program.

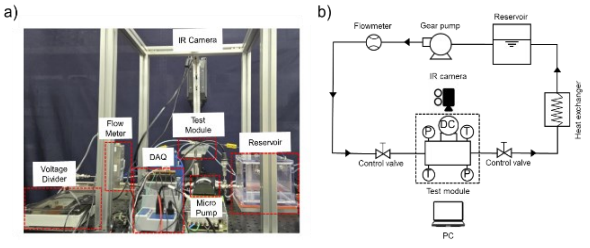

Fig. 5. Thermal–fluid performance measurement loop: (a) photograph of the experimental flow loop for device cooling evaluation; (b) schematic of the closed-loop system showing the micro pump, flow meter, pressure and temperature sensors, and an infrared camera used for non-contact junction temperature measurement.

2.3.2 Data reduction and uncertainty analysis

The electro thermal performance of the device was evaluated by systematically increasing the applied drain source voltage under fixed coolant flow rate conditions. The electrical power dissipated in the device, P_{diss}, was calculated as the product of the measured drain source voltage, V_{DS}, and drain source current, I_{DS}. The effective electrical resistance associated with device heating, R_{DS}, was determined from the measured V_{DS} and I_{DS} according to Ohm's law.

$$P_{diss}=I_{DS}\cdot V_{DS} \tag{1}$$

$$R_{DS}=\frac{V_{DS}}{I_{DS}} \tag{2}$$

The local heat flux generated within the device, q", was calculated by dividing P_{diss} by the defined active area. The active area, A_{act}, was defined as the product of the total gate width and the distance between the first and last gate fingers, yielding A_{act} = 2.3 × 0.1 mm^2, and was consistently applied in both the simulations and the experiments for the heat-flux calculation.

$$q''=\frac{P_{diss}}{A_{act}} \tag{3}$$

The total thermal resistance, R_{total}, was determined by dividing the temperature difference between the maximum junction temperature, $T_{j,max}$, and the coolant inlet temperature, $T_{f,in}$, by the applied heat flux. The total thermal resistance was further decomposed into conductive and convective components. The conductive thermal resistance, R_{cond}, was defined based on the temperature difference between $T_{j,max}$ and the average wall surface temperature, $T_{wall,avg}$. The convective thermal resistance, R_{conv}, represents the thermal resistance between $T_{wall,avg}$ and the ambient temperature, T_{amb}.

$$R_{total}=R_{cond}+R_{conv}=\frac{T_{j,max}-T_{f,in}}{q''} \tag{4}$$

$$R_{cond}=\frac{T_{j,max}-T_{wall,avg}}{q''} \tag{5}$$

$$R_{conv}=\frac{T_{wall,avg}-T_{amb}}{q''} \quad (6)$$

The pumping power required for coolant circulation, P_{pump}, was calculated as the product of the volumetric flow rate, Q, and the pressure drop, ΔP, across the package. To assess cooling efficiency relative to hydraulic power consumption, the coefficient of performance, COP, was defined as the ratio of P_{diss} to P_{pump}.

$$P_{pump}=\Delta P\times Q \quad (7)$$

$$COP=\frac{P_{diss}}{P_{pump}} \quad (8)$$

Measurement uncertainty was evaluated using standard error propagation based on instrument specifications. The uncertainty of the K-type thermocouples was ±1.1 °C and was applied to $T_{f,in}$ and $T_{f,out}$. The uncertainty of the infrared camera was ±2.0 % and was applied to $T_{j,max}$. The relative uncertainties of the differential pressure sensor and the Coriolis flow meter were ±0.5 % and ±0.3 % respectively. The uncertainty of the power supply was ±0.2 % and was applied to V_{DS} and I_{DS}. The tolerances of the voltage divider resistors and the shunt resistor were ±1.0 % and ±0.5 % respectively. Based on error propagation, the relative uncertainty of P_{pump} was calculated to be ±0.6 %. The relative uncertainty of the heat flux q" was calculated to be ±1.1 %. Over the operating range considered in this study, the uncertainty of the total thermal resistance R_{total} was estimated to be in the range of 2–8 %.

$$\left(\frac{U_{P_{pump}}}{P_{pump}}\right)^2=\left(\frac{U_{\Delta P}}{\Delta P}\right)^2+\left(\frac{U_Q}{Q}\right)^2 \quad (9)$$

$$\left(\frac{U_{q''}}{q''}\right)^2=\left(\frac{U_{V_D}}{V_D}\right)^2+\left(\frac{U_{I_D}}{I_D}\right)^2 \quad (10)$$

3. Result and discussion

The thermal fluid and electrical behavior of the packaged GaN-on-SiC HEMT was investigated through a combination of numerical analysis and experimental measurements. The thermal performance of the embedded cooling structure was

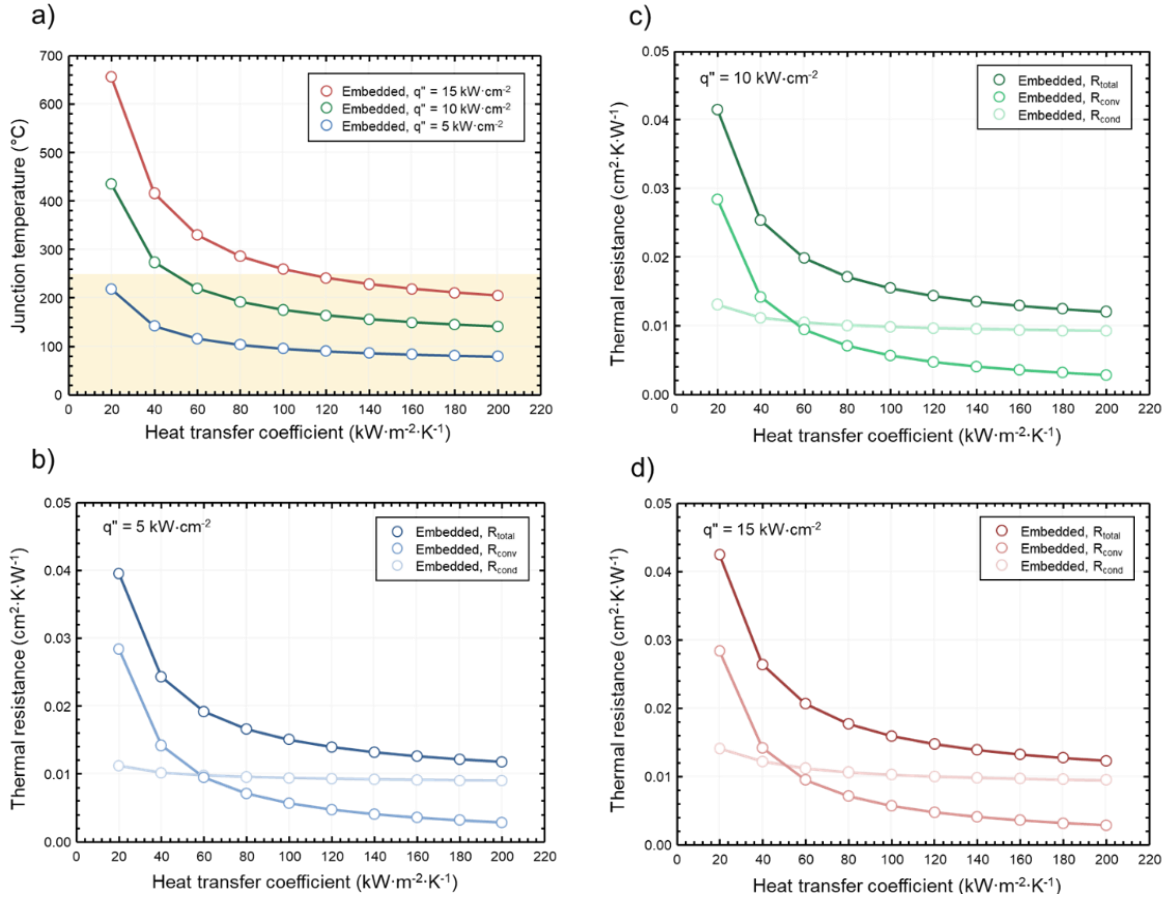

Fig. 6. Thermal response of the GaN-on-SiC device under varying heat flux and cooling conditions: (a) maximum junction temperature $T_{j,max}$ as a function of heat transfer coefficient; (b)-(d) total thermal resistance R_{total} and its conductive and convective components. The figure summarizes the dependence of junction temperature and thermal resistance on the heat transfer coefficient and reveals the increasing dominance of conductive thermal resistance at higher heat flux conditions.

evaluated in terms of junction temperature, heat flux, and thermal resistance under varying cooling conditions. Comparisons with a reference device employing conventional conduction cooling were used to isolate the impact of device level embedded cooling and TSV based integration.

3.1 Thermal–fluid characteristics of the embedded cooling structure

Fig. 6 summarizes the results of three dimensional steady state heat conduction analysis, illustrating the influence of the heat transfer coefficient on the maximum junction temperature $T_{j,max}$ and thermal resistance under different heat flux conditions. Fig. 6(a) shows the variation of $T_{j,max}$ as a function of the heat transfer coefficient for heat fluxes of 5 kW·cm^{-2}, 10 kW·cm^{-2}, and 15 kW·cm^{-2}. For all heat flux conditions, $T_{j,max}$ decreases monotonically with increasing heat transfer coefficient. In the low heat transfer coefficient regime, $T_{j,max}$ decreases rapidly, whereas the rate of reduction diminishes as the heat transfer coefficient increases. At a given heat transfer coefficient, higher heat flux conditions consistently result in higher $T_{j,max}$ values.

For GaN-on-SiC devices, the upper operational temperature limit is typically around 250 °C, while reliable long-term operation requires $T_{j,max}$ to be maintained below approximately 170 °C. To satisfy these temperature criteria, the required heat transfer coefficient increases with increasing heat flux. Under a heat flux of 15 kW·cm^{-2}, a heat transfer coefficient exceeding approximately 110 kW·m^{-2}·K^{-1} is required to maintain $T_{j,max}$ below the reliability threshold. In contrast, heat fluxes of 10 and 5 kW·cm^{-2} require heat transfer coefficients of approximately 50 and 10 kW·m^{-2}·K^{-1} respectively.

Figs. 6(b) through 6(d) show the variations of the total thermal resistance R_{total} and its conductive and convective components as functions of the heat transfer coefficient for the three heat flux conditions. Across all conditions, R_{total} decreases with increasing heat transfer coefficient. This reduction is primarily driven by the decrease in the convective thermal resistance R_{conv}, while the conductive thermal resistance R_{cond} remains nearly constant. As the heat transfer coefficient increases, R_{total} approaches an asymptotic value that reflects parasitic conduction resistance within the device structure. This behavior indicates that further enhancement of convective cooling yields diminishing reductions in overall thermal resistance once conduction limits are reached. As the heat flux increases from 5 to 15 kW·cm^{-2}, R_{total} increases modestly due to enhanced temperature nonuniformity and increased thermal spreading resistance, whereas R_{conv} remains relatively insensitive to heat flux under single phase cooling conditions.

3.2 Electro-thermal performance co-measurement

The electro thermal performance of the embedded cooling structure was experimentally evaluated by analyzing the relationship between junction temperature and heat flux under coolant flow rates of 15 and 25 mL·min^{-1}. Fig. 7 compares the thermal performance of the directly cooled device with that of a reference device packaged using a conventional CMC structure. Fig. 7(a) shows the variation of the maximum junction temperature $T_{j,max}$ as a function of heat flux. The reference device reaches its operational temperature limit of approximately 250 °C at a heat flux of 12.20 kW·cm^{-2}. In contrast, the directly cooled device maintains significantly lower junction temperatures across the same heat flux range. At a coolant flow rate of 15 mL·min^{-1}, $T_{j,max}$ is reduced to approximately 194 °C, while increasing the flow rate to 25 mL·min^{-1} further reduces $T_{j,max}$ to approximately 146 °C at comparable heat flux levels. Using 170 °C as the criterion for reliable operation, the allowable heat flux of the reference package is limited to 8.26 kW·cm^{-2}. Under the same junction temperature constraint, the embedded cooling structure sustains heat fluxes of 10.73 kW·cm^{-2} at 15 mL·min^{-1} and 14.41 kW·cm^{-2} at 25 mL·min^{-1}. This corresponds to an enhancement of approximately 30 % to 74 % in allowable heat flux, demonstrating the scalability of heat dissipation with increasing coolant flow rate.

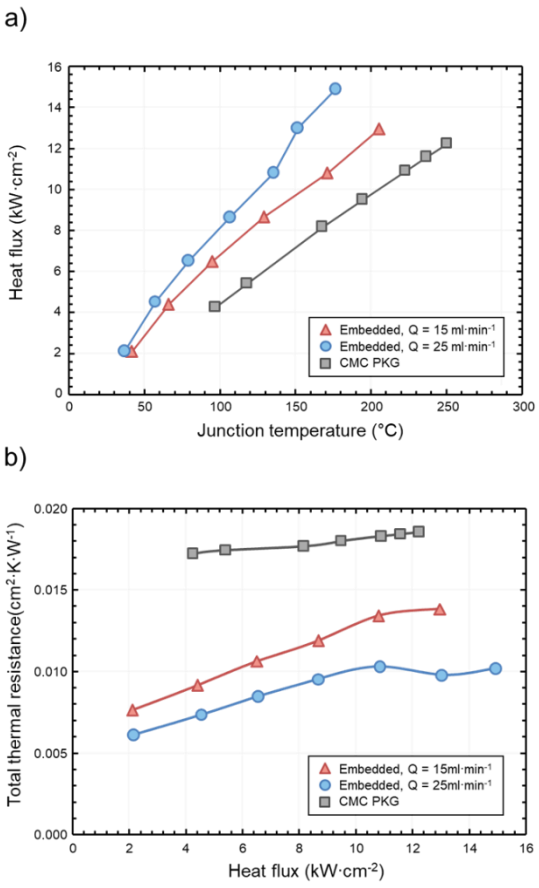

Fig. 7. Thermal performance of the embedded liquid cooling package: (a) junction temperature as a function of heat flux; (b) total thermal resistance as a function of heat flux. The figure compares the thermal response of the embedded liquid cooling package with that of a reference CMC package and shows the effect of coolant flow rate on junction temperature and thermal resistance.

Fig. 7(b) shows the variation of the total thermal resistance R_{total} as a function of heat flux. The reference package exhibits R_{total} values ranging from 0.017 to 0.018 $cm^2 \cdot K \cdot W^{-1}$ over the heat flux range of 4 to 12 $kW \cdot cm^{-2}$. In contrast, the embedded cooling structure exhibits substantially lower thermal resistance, with R_{total} values ranging from 0.0076 to 0.0138 $cm^2 \cdot K \cdot W^{-1}$ at 15 $mL \cdot min^{-1}$ and from 0.0061 to 0.0103 $cm^2 \cdot K \cdot W^{-1}$ at 25 $mL \cdot min^{-1}$. These results confirm that increasing coolant flow rate directly reduces thermal resistance and enables stable junction temperature control under high heat flux conditions.

Fig. 8 summarizes the relationship between pumping power, junction temperature, and cooling efficiency. Fig. 8(a) shows the variation of $T_{j,max}$ as a function of pumping power for different heat flux conditions. For a given coolant flow rate, $T_{j,max}$ increases with increasing heat flux and decreases with increasing flow rate. At fixed flow rates, a slight reduction in pumping power is observed as heat flux increases. This behavior is attributed to elevated coolant temperature and the associated reduction in fluid viscosity under higher heat dissipation conditions. At a heat flux of approximately 13 $kW \cdot cm^{-2}$, $T_{j,max}$ values of approximately 206 °C and 152 °C are achieved at coolant flow rates of 15 and 25 $mL \cdot min^{-1}$ respectively, while the corresponding pumping power remains in the range of 9 to 11 mW and 27 to 30 mW. These results demonstrate that substantial junction temperature reduction can be achieved with modest hydraulic power consumption.

Fig. 8(b) shows the variation of the coefficient of performance as a function of thermal resistance. The coefficient of performance increases with increasing heat flux, reflecting the combined effects of increased conductive thermal resistance and reduced pumping power at elevated coolant temperatures. This trend is more pronounced at lower coolant flow rates, where relative changes in coolant temperature have a stronger impact on fluid viscosity and pumping power. Over the operating range considered, the embedded cooling structure maintains R_{total} values on the order of 0.0061 to 0.0138 $cm^2 \cdot K \cdot W^{-1}$ while achieving high cooling efficiency.

Fig. 9 illustrates the influence of cooling conditions on the electrical output characteristics of the device. Fig. 9(a) shows the variations of drain current I_{DS} and junction temperature $T_{j,max}$ as functions of drain source voltage V_{DS} under different coolant

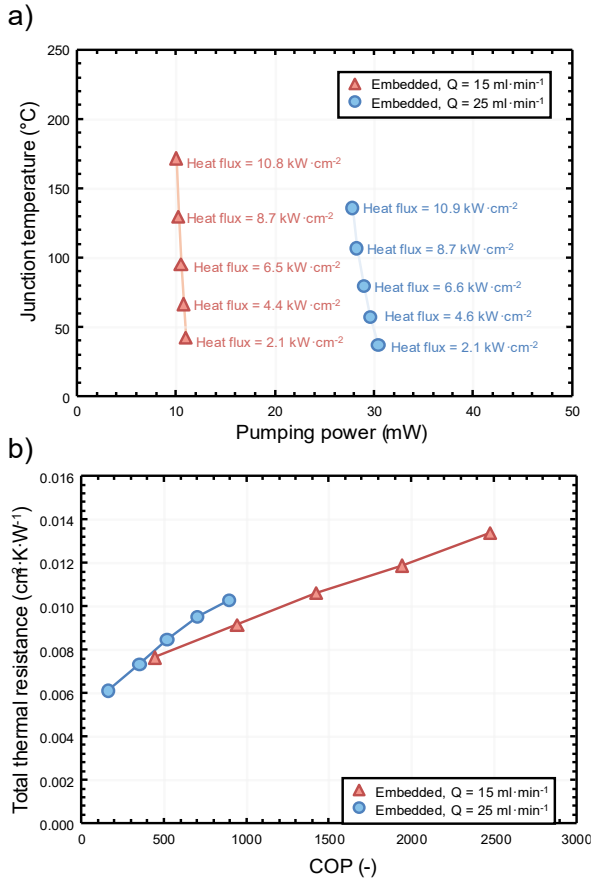

Fig. 8. Thermal–hydraulic performance of the package: (a) junction temperature as a function of pumping power; (b) coefficient of performance as a function of thermal resistance. The figure illustrates the relationship between pumping power, junction temperature and cooling efficiency, highlighting the influence of hydraulic operating conditions on system-level thermal performance.

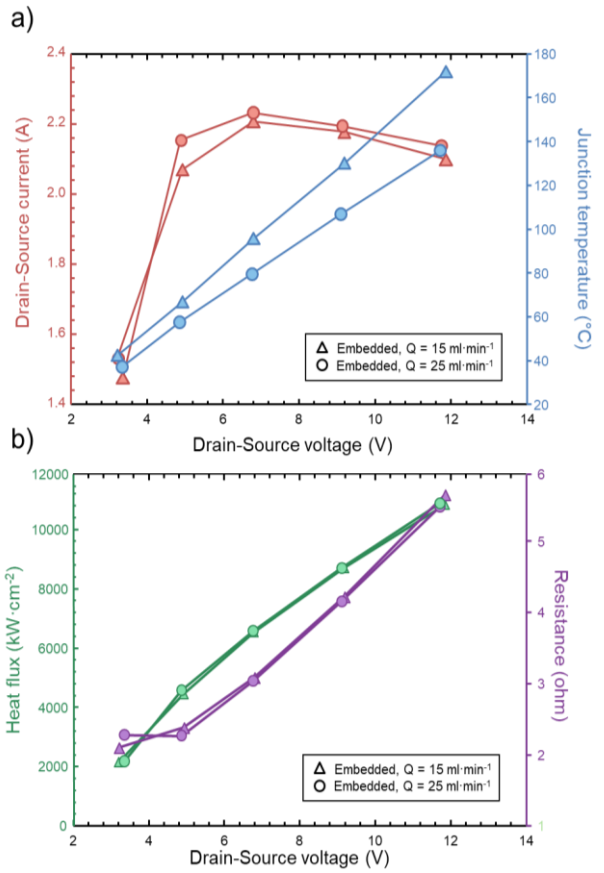

Fig. 9. Electrical output characteristics under different cooling conditions: (a) relationship between VDS, IDS, and $T_{j,max}$ for different coolant flow rates, illustrating the coupling between electrical operation and junction heating; (b) heat flux and RDS as a function of V_{DS}, highlighting the influence of cooling conditions on self-heating–induced resistance variation.

flow rates. As V_{DS} increases, I_{DS} initially increases rapidly and reaches saturation at approximately 2.1 A, while $T_{j,max}$ increases monotonically. At higher V_{DS}, I_{DS} decreases slightly from the saturation value as $T_{j,max}$ continues to increase. This behavior is attributed to self-heating induced degradation of carrier mobility. At identical V_{DS} values, higher coolant flow rates consistently result in lower $T_{j,max}$ and higher I_{DS}. In the saturation regime, increasing the coolant flow rate from 15 to 25 mL·min^{-1} increases I_{DS} by approximately 55 mA on average, demonstrating effective suppression of self-heating under enhanced cooling conditions.

Fig. 9(b) shows the variations of dissipated heat flux and the electrical resistance R_{DS} as functions of V_{DS}. Heat flux increases monotonically with increasing V_{DS}, accompanied by an increase in R_{DS} due to temperature dependent mobility degradation. At a given V_{DS}, higher coolant flow rates result in lower R_{DS} values. In the saturation voltage regime, R_{DS} measured at 25 mL·min^{-1} is approximately 0.2 to 0.3 Ω lower than that measured at 15 mL·min^{-1}. These results demonstrate that improved cooling directly mitigates self-heating effects and preserves electrical performance under high power operation.

4. Conclusions

In this work, a device level GaN-on-SiC HEMT architecture integrating direct liquid cooling and TSV based grounding within a single die was demonstrated and experimentally evaluated. By defining an embedded cooling channel beneath the source region and simultaneously establishing a low inductance electrical return path through TSVs, the proposed structure realizes a unified electro thermal pathway at the device level. This approach fundamentally differs from conventional packaging or interposer level integrations by eliminating additional thermal interfaces while directly coupling thermal management with RF relevant electrical behavior.

Compared with a reference conduction cooled device mounted in a CMC package, the proposed structure exhibits substantially enhanced thermal performance. At a junction temperature criterion of 170 °C, the reference device sustains a heat flux of 8.26 kW·cm^{-2}, whereas the embedded cooling structure achieves heat fluxes of 10.73 kW·cm^{-2}at a coolant flow rate of 15 mL·min^{-1} and 14.41 kW·cm^{-2} at 25 mL·min^{-1}, corresponding to an improvement of up to 74.4 %. The total thermal resistance is reduced to 0.0076 cm^2·K·W^{-1} at 15 mL·min^{-1} and further decreases to a minimum value of 0.0061 cm^2·K·W^{-1} at 25 mL·min^{-1}, confirming the effectiveness of direct device level liquid cooling.

The thermal improvements achieved by the embedded cooling structure are directly reflected in the electrical output characteristics of the device. Under identical bias conditions, enhanced cooling suppresses self-heating induced resistance increase and preserves carrier mobility, resulting in higher drain current and reduced electrical resistance at elevated operating voltages. These results demonstrate that thermal management and electrical performance are intrinsically linked at the device level and cannot be independently optimized in high power GaN RF electronics.

Overall, this work establishes TSV defined embedded cooling as a practical and scalable strategy for device level electro thermal co-design in high power density GaN HEMTs. The demonstrated architecture provides a clear pathway toward simultaneous enhancement of thermal reliability and electrical performance, and offers important design guidance for next generation millimeter wave RF and power electronic systems requiring aggressive power density scaling.

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Conflict of interest

The authors declare no competing interests.

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