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Fundamental conduction cooling limits for sub-1 μm Ga_2O_3 devices integrated with diamond

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ABSTRACT

Beta-phase gallium oxide (β-Ga_2O_3), as an ultrawide bandgap semiconductor, is promising for next generation power and radio frequency electronics. Its low thermal conductivity, however, poses a challenge to thermal management of devices composed of it, causing a reduced power performance as well as temperature-induced reliability problems. Several recent efforts have focused upon the impact of various device-level thermal management approaches, including integration with high-thermal-conductivity substrates (e.g., diamond and SiC) as a bottom-side passive heat extraction method, on the cooling performance of β-Ga_2O_3 devices. These efforts, however, have been restricted to cases where the Ga_2O_3 layer thicknesses are above 1 μm. Here, we address the fundamental conduction cooling limits for sub-1 μm β-Ga_2O_3 devices integrated with diamond via finite element simulations. A semi-classical transport theory for phonons interacting with interfaces is employed to systematically calculate the thickness-dependent thermal conductivity of the β-Ga_2O_3 layers with different crystallographic orientations for both cross-plane and in-plane directions. We find that the maximum power density of sub-1 μm β-Ga_2O_3 devices on diamond, particularly that of the 0.1 μm device, can reach up to 7.7 W mm^{-1} with a junction temperature limit of 200 °C, considering an optimal device orientation as well as best-case experimental Ga_2O_3/diamond thermal boundary conductance (TBC). As the Ga_2O_3/diamond TBC approaches the limit predicted by the diffuse mismatch model, the fundamental limit to the maximum power density of these devices can reach up to 8.6 W mm^{-1}, which is comparable to those reported previously for costly augmented thermal management designs. Our findings suggest that the integration with diamond can fundamentally enhance the device-level cooling performance of Ga_2O_3 electronics, sub-1 μm devices in particular, and has thereby the potential to significantly reduce system-level cooling costs and packaging challenges.

1. Introduction

Beta-phase gallium oxide (β-Ga_2O_3) has recently begun to garner considerable attention for next-generation power electronics applications due to its outstanding electrical properties, such as an ultrawide bandgap (~4.8 eV) and a high critical breakdown electric field (~8 MV cm^{-1}) [1–3]. Because of these superior properties, β-Ga_2O_3 has exceptionally higher figures of merit that are relevant to high-power and high-frequency applications, when compared to those of wide bandgap materials such as 4H-SiC and GaN [1–3]. Baliga's figure of merit (BFOM) of β-Ga_2O_3 is a factor of 10 and 4 higher than those of 4H-SiC and GaN, respectively, owing to the cubic power dependence of BFOM on the critical electric field [1–3]. Its Johnson's figure of merit (JFOM), which represents the power-frequency product for radio-frequency (RF) amplification, is a factor of 3 higher than that of GaN [3]. These higher figures of merit, combined with the commercial availability of low-cost large-size single-crystal native β-Ga_2O_3 substrates synthesized using melt-growth techniques [3,4], render β-Ga_2O_3 a promising material for high voltage switching and RF electronics applications [5–7].

However, the thermal conductivity of bulk β-Ga_2O_3 (11–27 W m^{-1} K^{-1}, depending on its crystallographic direction, at room temperature [8,9]) is one order of magnitude lower than those of wide bandgap counterparts (e.g., ~230 and ~350 W m^{-1} K^{-1} for bulk GaN and 4H-SiC, respectively, at room temperature [10–12]). Its lower intrinsic thermal conductivity can significantly exacerbate device-level self-heating effects, resulting in even higher device junction temperatures when compared to those in wide bandgap counterparts [13–16]. For example, a recent simulation work pre-

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dicted an exceptionally high junction temperature rise of ~1500 °C for a typical β-Ga_2O_3 metal-oxide-semiconductor field-effect transistor (MOSFET)—whose device layer is homoepitaxially grown on a native substrate—at a power density of 10 W mm^{-1} [15]. Another recent study on a similar β-Ga_2O_3 MOSFET measured a thermal resistance of 88 mm K W^{-1} at 1.87 W mm^{-1} power density (which can be converted to a junction temperature rise of ~165 °C at this power density), which is a factor of 6 larger than that of a multi-finger GaN high-electron-mobility transistor (HEMT) with similar gate dimensions on a SiC substrate [14]. The high device junction temperature can severely limit device performance and degrade device reliability [6,7]. Since heat dissipation in β-Ga_2O_3-based devices is a primary concern, increasing attention has recently been paid to their thermal characteristics and thermal management [13–16], although still much less explored than their electrical characteristics.

The thermal management of β-Ga_2O_3 devices can heavily benefit from a number of thermal management solutions that have been extensively developed for GaN HEMTs over the past decade [11,17,18]. These solutions can be grouped broadly into two categories: bottom-side and top-side cooling schemes. The former includes the heterogeneous integration of GaN with high-thermal-conductivity diamond (as high as ~2000 W m^{-1} K^{-1} [19]) near the device junction to form GaN-on-diamond [11,20–24] and the use of microchannel liquid cooling to enhance convective heat transfer [17,18,25–28]. The latter includes the use of a heat-spreading capping layer (e.g., nanocrystalline diamond) on top of the device layers [29,30]. Among these approaches, the GaN-diamond integration approach has been proven to fundamentally improve the near-junction conduction cooling of GaN HEMTs [11,18,31]. The key is to bring the superior heat spreading capability of the diamond substrate in close proximity of the heat generating region of the device (i.e., the device junction).

Similar to the GaN-diamond integration approach, recent efforts have heterogeneously integrated β-Ga_2O_3 thin films on high-thermal-conductivity substrates (diamond and SiC) for the purpose of improving the near-junction conduction cooling of β-Ga_2O_3 devices [32–36]. These efforts can be classified into two groups. The first approach involves transfer and bonding of β-Ga_2O_3 thin films to high-thermal-conductivity substrates. For instance, Noh et al. [32] mechanically exfoliated β-Ga_2O_3 membranes with thicknesses from 50 to 150 nm from a bulk single crystal, transferred them onto a single crystal diamond substrate, and demonstrated that β-Ga_2O_3 devices on diamond exhibit ~60% lower channel temperature rise than a device on a sapphire substrate. Likewise, Cheng et al. [33] fabricated a mechanically exfoliated β-Ga_2O_3 membrane with a thickness of 427 nm on a single crystal diamond and showed by thermal simulation that the maximum temperature rise of the β-Ga_2O_3 device on diamond can be significantly lower than those of the devices on SiC and Si. Thin film β-Ga_2O_3 bonded to SiC was also realized by Cheng et al. [34], where ion-cutting and surface-activated bonding techniques were used to heterogeneously integrate wafer-scale single-crystalline β-Ga_2O_3 thin films (139–165 nm) onto 4H-SiC substrates. The second approach involves direct growth of Ga_2O_3 thin films on high-thermal-conductivity substrates [35,36]. One example is nanocrystalline β-Ga_2O_3 thin films, with thicknesses ranging from 28 to 115 nm, grown by atomic layer deposition (ALD) directly on single crystal diamond substrates [35]. Another example is an 81-nm-thick β-Ga_2O_3 thin film grown by molecular beam epitaxy on a 4H-SiC substrate [36].

Along with these integration efforts, increasing attempts have been made to measure the thermal conductivity of β-Ga_2O_3 in both bulk and thin film forms [8,9,33–37], as well as the thermal boundary resistance (TBR), which is the inverse of the thermal boundary conductance (TBC), between β-Ga_2O_3 and high-thermal-conductivity substrates [33–36]. Utilizing the thermal properties obtained from these measurements, several previous works using thermal simulation have investigated the heat dissipation performance of β-Ga_2O_3 devices on high-thermal-conductivity substrates, in particular, that of β-Ga_2O_3-on-diamond devices [15,16]. Chatterjee et al. [15] examined the heat dissipation performance of β-Ga_2O_3 devices (on native Ga_2O_3 substrates thinned down to 10 and 100 μm) integrated with a diamond substrate, and showed that the thermal resistance of the 10 μm device is ~5× lower than that of the 100 μm device. A similar study was performed by Yuan et al. [16], where a factor of 5 reduction in the device thermal resistance was reported with decreasing Ga_2O_3 thickness from 100 to 1 μm. Despite these simulation results, the cooling performance of sub-1 μm Ga_2O_3 devices integrated with diamond has not been systematically studied yet. In the aforementioned integration approaches with high-thermal-conductivity substrates, the Ga_2O_3 layer thicknesses are less than 1 μm (down to ~100 nm), where the phonon mean free paths become comparable to the layer thickness [38]. The size effect is thus expected to be prominent as a consequence of phonon-boundary scattering. It is therefore essential to consider the thermal conductivity of the Ga_2O_3 layer as a function of layer thickness for both cross-plane and in-plane directions when accurately assessing the device-level heat dissipation performance of sub-1 μm Ga_2O_3 devices. However, most previous simulation works considered the Ga_2O_3 layer thicknesses above 1 μm and assumed the bulk Ga_2O_3 thermal conductivity [7,14–16,39].

In this work, we explore the fundamental conduction cooling limits for sub-1 μm β-Ga_2O_3 devices integrated with diamond. By employing a semi-classical phonon transport model, we systematically calculate the thickness-dependent thermal conductivity of the β-Ga_2O_3 layers with different crystallographic orientations for both cross-plane and in-plane directions. Exploiting these calculations together with finite element simulations, we examine the conduction cooling performance of sub-1 μm β-Ga_2O_3 devices on diamond and assess their peak power density that may be feasible with a junction temperature limit of 200 °C. Our simulation results indicate that sub-1 μm β-Ga_2O_3 devices on diamond, particularly the 0.1 μm device, can achieve a maximum power density as high as 7.7 W mm^{-1}, assuming an optimal device orientation as well as best-case experimental Ga_2O_3/diamond TBC. The fundamental limit to the maximum power density of these devices can reach up to 8.6 W mm^{-1} as the Ga_2O_3/diamond TBC approaches the upper limit predicted by the diffuse mismatch model. The outcomes of this work suggest that the integration of sub-1 μm β-Ga_2O_3 devices with diamond has the potential to fundamentally increase the device power handling capability without requiring additional cooling components and complexity associated with costly augmented thermal management designs.

2. Simulation methodology

2.1. Finite-element thermal model

Conduction cooling of β-Ga_2O_3 devices on diamond is investigated by performing finite element analysis using COMSOL Multiphysics. As depicted in Fig. 1, we construct a 3D finite element device thermal model, the geometry and dimensions of which are mostly adopted from Ref. [16], and determine steady-state temperature fields of the model by solving the steady-state heat diffusion equation. The Ga_2O_3-on-diamond device structure employed in this work consists of a Ga_2O_3 layer with varying thickness (d) from 0.1 to 1 μm on a 2-mm-thick diamond substrate (Fig. 1(a)). In order to evaluate the conduction cooling performance of sub-1 μm Ga_2O_3 devices on diamond, thicker Ga_2O_3 layer thicknesses of 2, 5, and 10 μm are also considered in our simulation for comparison.

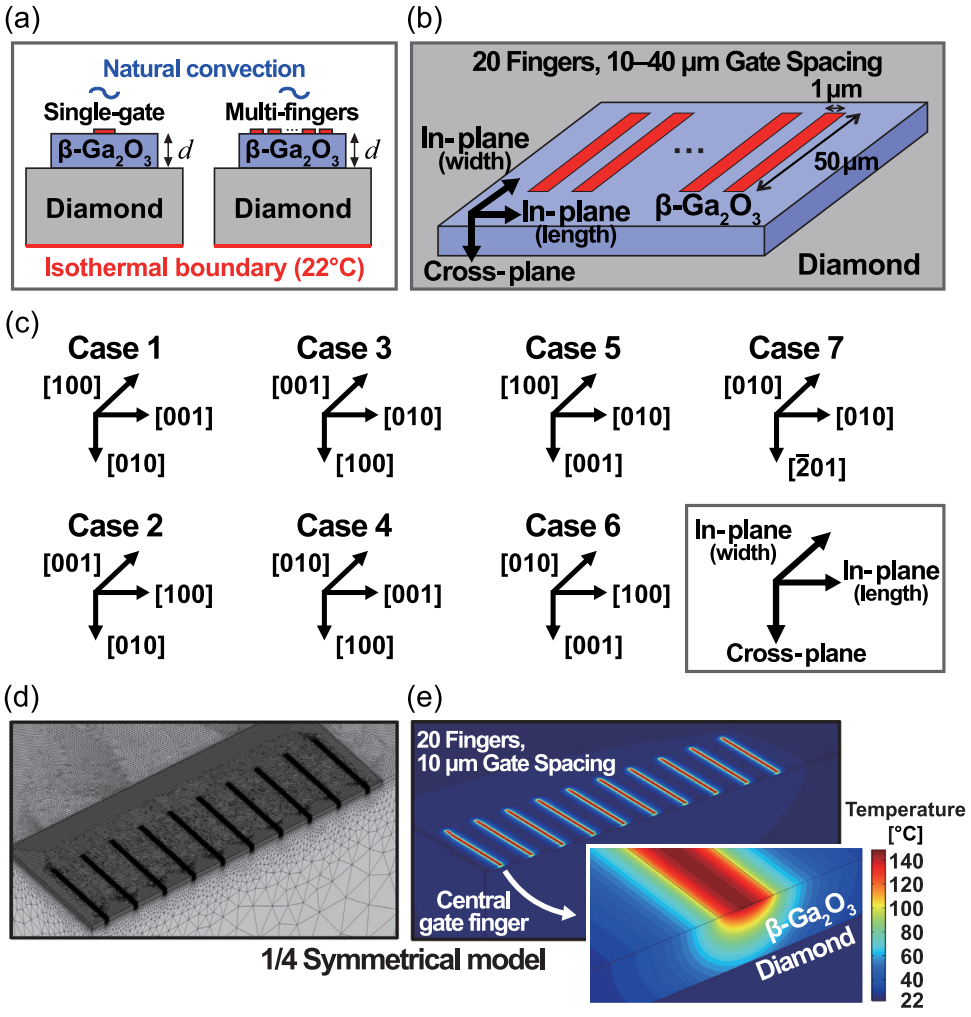

Fig. 1. (a) Cross-sectional schematic of the β-Ga_2O_3-on-diamond device thermal model employed in our current study (not drawn to scale). A heat generation region in single-gate and multi-finger devices is modeled by a single surface heater and an array of multiple surface heaters, respectively. (b) 3D Schematic of the multi-finger β-Ga_2O_3-on-diamond device model with 20 fingers and 10–40 μm gate pitch (not drawn to scale). The length and width of each heater are 1 and 50 μm, respectively. In-plane (both along the heater length and width) and cross-plane directions are presented in reference to the model. (c) Seven possible crystallographic orientations of the β-Ga_2O_3 layer considered in our model, depending on whether the [010] direction with the highest thermal conductivity is oriented along the cross-plane or in-plane direction. (d) Representative finite element mesh and (e) 3D steady-state temperature profile for the multi-finger β-Ga_2O_3-on-diamond model geometry shown in (a) and (b). The finest mesh elements are placed near the heat sources where Joule heating is concentrated. Quarter-symmetry is exploited here to reduce the computational expense.

As a heat source, single-gate and multi-finger device models utilize a single heater and an array of multiple heaters, respectively, on top of the Ga_2O_3 layer (Fig. 1(a)). For the latter, we consider 20 fingers and 10–40 μm gate pitch.

We also vary the crystallographic orientation of the β-Ga_2O_3 layer in the model and examine its impact on the cooling performance of β-Ga_2O_3 devices on diamond. Fig. 1(b) illustrates the two in-plane directions (along the heater length and width), as well as the cross-plane direction of the model. We consider seven possible cases, as seen in Fig. 1(c), depending on whether the crystal direction of β-Ga_2O_3 with the highest thermal conductivity, i.e., the [010] direction, is oriented along the cross-plane or in-plane direction. For Case 1, the [010] direction is aligned along the cross-plane direction with [001] and [100] directions along the in-plane directions (the directions of heater length and width, respectively). Case 2 also assumes [010] along the cross-plane direction but the lateral plane is rotated by 90° with respect to that in Case 1. Cases 3 and 4 assume the [010] direction along the heater length and width, respectively, with [100] being aligned along the cross-plane direction. Likewise, the [010] direction is oriented along the heater length and width for Cases 5 and 6, respectively, while the [001] direction is assumed along the cross-plane direction for both cases. For Case 7, the [$\bar{2}$01] direction is aligned along the cross-plane direction and the [010] direction is assumed along both the heater length and width directions, setting an upper performance limit of ($\bar{2}$01)-oriented β-Ga_2O_3 devices.

It is of note that a majority of lateral β-Ga_2O_3 field-effect transistors (FETs) have been fabricated on (010)-oriented Ga_2O_3 substrates with the [001] direction aligned along the gate length [7,13,14,16], corresponding to Case 1. Cases 3 and 4 correspond to the orientation of recently demonstrated β-Ga_2O_3 FETs on diamond [32,33], where (100)-oriented Ga_2O_3 nanomembranes were mechanically exfoliated and then adhered to single crystal diamond. Case 5 is directly taken from Ref. [40], where vertical MOSFETs were implemented on (001)-oriented Ga_2O_3 substrates. Case 7 is the configuration from Ref. [15], where a lateral Ga_2O_3 MOSFET was constructed on a ($\bar{2}$01)-oriented Ga_2O_3 substrate.

As a benchmark, we also consider β-Ga_2O_3 devices on SiC by replacing the diamond substrate in the model with SiC. The crystallographic orientation of the β-Ga_2O_3 layer is assumed to be those of Cases 1 and 7. These are based on recent Ga_2O_3-SiC integration practices [34,36,39,41]. One approach has used a fusion

bonding technique to fabricate a Ga_2O_3/4H-SiC composite wafer by integrating a (010)-oriented β-Ga_2O_3 wafer with a 4H-SiC wafer [39,41]. Other approaches have demonstrated $(\bar{2}01)$ β-Ga_2O_3 thin films bonded to 4H-SiC [34], as well as a $(\bar{2}01)$ β-Ga_2O_3 thin film epitaxially grown on 4H-SiC [36].

Our thermal model seeks to consider a generic case for lateral Ga_2O_3 devices and therefore make three simplifying assumptions. First, we ignore the existence of the gate, source, and drain electrodes, as well as the channel and barrier layers, for the sake of simplicity. As we discuss in Sec. S2(c) of Supplementary Material, the influence of this assumption on the maximum device temperature is not significant, suggesting that the majority of the heat generated in the device active region propagates downwards into the Ga_2O_3 layer, Ga_2O_3/diamond interface, and diamond substrate. As quantified in Fig. S9 of Supplementary Material, the addition of the metal electrodes as well as the channel and barrier layers can result in an ~10% difference in the maximum device temperature, when compared to our current simplified model, which can be attributed to additional heat dissipation pathways formed by the high-thermal-conductivity metal electrodes. Our quantification is consistent with that made previously by Pomeroy et al. [14], where a 14% increase in device thermal resistance was predicted by removing gold electrodes in their finite element thermal model for β-Ga_2O_3 MOSFETs. Second, a surface heat source is applied as either a single rectangular strip or an array of rectangular strips (Figs. 1(a) and (b)), which represents the heat generation region of single-gate and multi-finger devices, respectively, as previously assumed for lateral GaN and Ga_2O_3 devices by a number of works [11,18,22,31,33,42,43]. The length and width of each heater are assumed to be 1 and 50 μm, respectively, taken from Ref. [16], which represent the dimensions of an actual hotspot of each gate finger. We note that the heat generation in lateral Ga_2O_3 devices is typically volumetric and concentrated near the drain side edge of the gate [15,16]. It is also of note that several factors, including device geometry and bias conditions, can influence the internal heat generation profile [39,44]. Third, the spreading and heat sink beneath the substrate (diamond or SiC) is assumed to operate ideally, and thereby the bottom of the substrate is set to a fixed temperature of 22 °C, as in several previous studies for lateral GaN and Ga_2O_3 devices [16,22,31,33,42]. While this may represent fairly aggressive system-level and packaging requirements [15,16,18], one of our current goals is to understand the general trends in device-level heat dissipation of sub-1 μm Ga_2O_3 devices on diamond.

Given the symmetric nature of the device structure, a quarter-symmetry model (Figs. 1(d) and (e)) is utilized here with adiabatic boundary conditions imposed on its inner surfaces to reduce the computational load. Except the bottom surface of the substrate (diamond or SiC), all other exterior surfaces are subjected to natural convection with the heat transfer coefficient of 10 W m^{-2} K^{-1} and the ambient temperature of 22 °C [16]. The dissipated power density (P) is set to 1.8 W mm^{-1} as a baseline value and then varied to match the maximum device temperature of 200 °C, which has been previously established by Refs. [15,16] as a safe junction temperature limit for the reliable long-term operation of devices.

A progressive tetrahedral mesh is implemented to discretize the simulation domain, as sketched in Fig. 1(d). The finest and highest density mesh elements are located in the close vicinity of the heat generation region, with minimum mesh sizes of 25, 40, and 60 nm for the Ga_2O_3 layer thicknesses of 0.1, 1, and 10 μm, respectively, to accurately capture large temperature gradients around the heat sources. The density of mesh elements is gradually decreased with increasing distance from the heat generation region in both the cross-plane and in-plane directions. Our simulation employs 18 to 25 million mesh elements, which depend on the thickness of the Ga_2O_3 layer. Mesh convergence tests are performed to ensure the convergence of the finite element calculations. A representative mesh convergence plot for the single-gate Ga_2O_3-on-diamond device model is provided in Fig. S8 of Supplementary Material. A representative 3D steady-state temperature profile of the multi-finger Ga_2O_3-on-diamond device model is shown in Fig. 1(e), where the Ga_2O_3 layer thickness is 1 μm, the gate pitch is 10 μm, the Ga_2O_3/diamond thermal boundary conductance is 20 MW m^{-2} K^{-1}, and the crystal orientation corresponds to Case 1. An inset of Fig. 1(e) clearly shows that the temperature drop is significant within the Ga_2O_3 layer, while that within the diamond substrate is negligible.

Heterogeneous integration of sub-micrometer-thick β-Ga_2O_3 devices with diamond substrates has been barely realized, to our knowledge. This makes it tricky to compare our simulation results, particularly focusing on sub-micrometer β-Ga_2O_3 devices on diamond, with experimental results available in the literature. Instead, we choose to validate our finite element device thermal model using temperature measurements performed on homoepitaxial β-Ga_2O_3 devices, where the device layer is homoepitaxially grown on a native substrate. We take an example of an $(Al_{0.19}Ga_{0.81})_2O_3/Ga_2O_3$ modulation-doped field effect transistor (MODFET) [39] and compare experimentally measured surface temperature rises of this device, taken from Ref. [39], with predictions of our model. Greater details of this comparison can be found in Sec. S2(a) of Supplementary Material.

2.2. Thermal properties

The thermal properties of both Ga_2O_3-on-diamond and Ga_2O_3-on-SiC device structures are given as inputs to our finite element device thermal model. These encompass the thermal conductivity of the β-Ga_2O_3 layer ($k_{Ga_2O_3}$), the thermal boundary conductance (TBC) between the β-Ga_2O_3 layer and the diamond substrate and between the β-Ga_2O_3 layer and the SiC substrate, and the thermal conductivity of the diamond and SiC substrates (k_{Diam} and k_{SiC}, respectively). As discussed later in greater details in Section 2.3, we systematically calculate cross-plane and in-plane $k_{Ga_2O_3}$ as a function of Ga_2O_3 layer thickness and temperature for all cases (Fig. 1(c)) described in Section 2.1. The values of the Ga_2O_3/diamond and Ga_2O_3/SiC TBCs, as well as k_{Diam} and k_{SiC}, are taken from previous reports in the literature [10,33–36,43], as discussed below.

Among a wealth of literature on the thermal conductivity of diamond in both bulk and thin film forms [19,43,45,46], k_{Diam} is assumed to be 2158 W m^{-1} K^{-1} at room temperature with its temperature dependence of T^{-1}, directly taken from a previous measurement on high-purity single-crystal bulk diamond [43], since state-of-the-art Ga_2O_3-on-diamond integration practices [32,33,35] have integrated Ga_2O_3 thin films onto single crystal diamond. Although there exist a few experimental reports on the Ga_2O_3/diamond TBC [33,35], these prior findings indicate a range of experimental values from 17 to 179 MW m^{-2} K^{-1}. Using time-domain thermoreflectance (TDTR), Cheng et al. [33] measured the room-temperature TBC to be 17 MW m^{-2} K^{-1} for a Ga_2O_3 nanomembrane adhered to single crystal diamond via van der Waals interactions. Another TDTR study [35] determined the TBC to be 136–179 MW m^{-2} K^{-1} at room temperature for atomic-layer-deposited Ga_2O_3 films on single crystal diamond. Based on these previous experimental reports, a range of TBC values from 20 to 180 MW m^{-2} K^{-1} is assumed as the Ga_2O_3/diamond TBC in our Ga_2O_3-on-diamond device model.

The thermal conductivity of the SiC substrate (k_{SiC}) is assumed to be anisotropic with $330(T/300)^{-1.49}$ and $500(T/300)^{-1.49}$ W m^{-1} K^{-1} along the cross-plane and in-plane directions, respectively, taken from Ref. [10]. A few experimental reports on the Ga_2O_3/SiC TBC exist with values ranging from 67 to 142 MW m^{-2} K^{-1} [34,36]. A previous TDTR measurement [34] reported the Ga_2O_3/SiC TBC

to be approximately 67–99 MW m^{-2} K^{-1} at room temperature for β–Ga_2O_3 thin films (139–165 nm) bonded to 4H-SiC. Nepal et al. [36] also used TDTR and reported the Ga_2O_3/SiC TBC of 142 MW m^{-2} K^{-1} at room temperature for a β–Ga_2O_3 thin film (81 nm) epitaxially grown on 4H-SiC. Based on these previous measurements, a range of TBC values from 70 to 140 MW m^{-2} K^{-1} is assumed as the Ga_2O_3/SiC TBC in our Ga_2O_3-on-SiC device model.

2.3. Ga_2O_3 thermal conductivity

The thermal conductivity of β-Ga_2O_3 is highly anisotropic, depending on its crystallographic direction, due to its monoclinic lattice structure and low crystal symmetry [8,9]. We calculate the anisotropic thermal conductivity of β-Ga_2O_3 along principal crystallographic directions (i.e., [100], [010], [001], and [$\bar{2}$01] directions) by using a semi-classical phonon transport model [21,47–49]. In this approach, the thermal conductivity is written as

$$k = \frac{1}{6\pi^2}\sum_j \int_q \frac{\hbar^2\omega_j^2(q)}{k_B T^2}\frac{\exp\left[\frac{\hbar\omega_j(q)}{k_B T}\right]}{\left(\exp\left[\frac{\hbar\omega_j(q)}{k_B T}\right]-1\right)^2} v_{g,j}^2(q)\tau_j(q,T)q^2 dq, \quad (1)$$

where q is the wavevector, $\hbar$ is the reduced Planck's constant, k_B is the Boltzmann constant, and ω, $v_g = \partial\omega/\partial q$, and τ are the angular frequency, group velocity, and scattering time of phonons, respectively, at temperature T. The subscript j denotes the acoustic phonon branch. We model the dispersion of the three acoustic phonon branches for each crystallographic direction with the Born-von Karman dispersion [21,22,47,48], where $\omega_j = \omega_{0,j}\sin(\pi q/2q_0)$. Here, $q_0 = (6\pi^2\eta)^{1/3}$ is the Debye cutoff wavevector with $\eta = 9.58 \times 10^{27}$ m^{-3} [50] being the number density of primitive cells. $\omega_{0,j} = 2v_{s,j}q_0/\pi$ is the highest phonon frequency at the first Brillouin zone edge and $v_{s,j}$ is the sound velocity of each branch, taken from Ref. [8].

Our analytical model considers the Umklapp phonon-phonon scattering process, $\tau_{U,j}^{-1} = BT\omega_j^2(q)\exp(-C/T)$, the phonon-impurity scattering process, $\tau_{I,j}^{-1} \sim \Gamma\omega_j^4(q)$, and the phonon-boundary scattering process, $\tau_{B,j}^{-1} = v_{g,j}(q)/L$. Here, Γ is the parameter to describe the phonon scattering strength due to point defects and L is the characteristic dimension of the sample. These three scattering mechanisms are combined via Matthiessen's rule to yield the total scattering rate: $\tau_j^{-1} = \tau_{U,j}^{-1} + \tau_{I,j}^{-1} + \tau_{B,j}^{-1}$. To treat the phonon-impurity scattering, we focus on the scattering strength arising from Sn, a typical dopant for β-Ga_2O_3 [1,8,40,51,52]. It is worth noting that the parameter Γ also includes scattering effects from isotopes of each constituent element; i.e., mass disorder introduced by isotopes can scatter phonons and thus impede heat transfer [12,53]. The strength of the phonon-isotope scattering in β-Ga_2O_3 is calculated to be 2.76 $\times 10^{-4}$, consistent with that reported previously by Tran et al. [51]. Further details on our treatment of the phonon-impurity scattering are provided in Sec. S1(a) of Supplementary Material. Choosing B and C as adjustable parameters, we fit the thermal conductivity model to the temperature-dependent thermal conductivity data of bulk β-Ga_2O_3 for each crystallographic direction in the temperature range of 220–500 K [8]. This yields $B = 12.64 \times 10^{-19}$ s K^{-1}, $C = 74.7$ K for the [100] direction, $B = 6.59 \times 10^{-19}$ s K^{-1}, $C = 134.2$ K for the [010] direction, $B = 9.78 \times 10^{-19}$ s K^{-1}, $C = 76.8$ K for the [001] direction, and $B = 11.28 \times 10^{-19}$ s K^{-1}, $C = 77.3$ K for the [$\bar{2}$01] direction. Further discussions on the Umklapp scattering parameters and relaxation times for the four different crystallographic directions are provided in Sec. S1(b) of Supplementary Material.

Our objective here is to predict the lattice thermal conductivity of β-Ga_2O_3 thin films with different crystallographic orientations as a function of film thickness for both cross-plane and in-plane directions. It was previously estimated using first-principles calculations that the mean free paths of phonons in bulk β-Ga_2O_3 range from several nanometers to several micrometers [38]. Sub-micrometer-thick Ga_2O_3 films thus possess lower thermal conductivity than bulk Ga_2O_3 due to the size effect stemming from phonon-boundary scattering. Moreover, even for an isotropic crystal, phonons traveling perpendicular to the film can be scattered more frequently by the film boundaries than those moving parallel to the film [54]. To capture these aspects, we implement a heat flux suppression function S on the bulk phonon scattering rate term, rather than using the aforementioned boundary scattering expression, for both cross-plane and in-plane directions; i.e., $\tau_j = S\tau_{bulk,j}$, where $\tau_{bulk,j}^{-1} = \tau_{U,j}^{-1} + \tau_{I,j}^{-1}$. These suppression functions are based on solutions to the Boltzmann transport equation for cross-plane and in-plane heat flow in a thin film, respectively. We use the Fuchs-Sondheimer formula [55,56] as the suppression function for in-plane heat conduction. This theory has been extended to the cases of spectral-dependent phonon-boundary scattering [49], and the suppression function for the in-plane thermal conductivity, S_{IP}, can be expressed as

$$S_{IP}(\mathrm{Kn}) = 1 - \frac{3}{8}\mathrm{Kn}\left[1 - 4E_3\left(\mathrm{Kn}^{-1}\right) + 4E_5\left(\mathrm{Kn}^{-1}\right)\right], \quad (2)$$

under the assumption that phonon-boundary scattering is purely diffuse. Here, $\mathrm{Kn}(q,T) = \Lambda_{bulk}/d$ is the Knudsen number, where $\Lambda_{bulk,j} = \tau_{bulk,j}v_{g,j}$ is the bulk phonon mean free path and d is the film thickness. $E_n(x)$ is the nth-order exponential integral function [57], written as

$$E_n(x) = \int_0^1 \mu^{n-2}\exp\left(-\frac{x}{\mu}\right)d\mu. \quad (3)$$

In order to predict the cross-plane thermal conductivity, we introduce the simplified suppression function proposed by Hua et al. [57] into our model, which is given by

$$S_{CP}(\mathrm{Kn}) = 1 + 3\mathrm{Kn}\left[E_5\left(\mathrm{Kn}^{-1}\right) - \frac{1}{4}\right]. \quad (4)$$

3. Results and discussion

Fig. 2 shows the cross-plane thermal conductivity of (010)- and ($\bar{2}$01)-oriented β-Ga_2O_3 thin films versus film thickness (d) at room temperature, incorporating the predictions of our model [Eqs. (1) and (4)], represented by green and black solid slides, respectively, as well as the best available data from the literature. The latter are from Ref. [41] (triangles), where 10.1–19.0 W m^{-1} K^{-1} were measured using TDTR for 2.7–6.5 μm (010) β-Ga_2O_3 films that were thinned from a Ga_2O_3/4H-SiC composite wafer, Ref. [34] (red diamonds), where 2.9–6.1 W m^{-1} K^{-1} were measured using TDTR for 139–165 nm ($\bar{2}$01) β-Ga_2O_3 films bonded to 4H-SiC, Ref. [36] (blue squares), where 3.1–3.2 W m^{-1} K^{-1} were measured using TDTR for 81–120 nm ($\bar{2}$01) β-Ga_2O_3 films grown by molecular beam epitaxy on 4H-SiC and c-plane sapphire, and Ref. [51] (yellow circles), where 2.5–5.4 W m^{-1} K^{-1} were measured using nanosecond transient thermoreflectance for 245–255 nm ($\bar{2}$01) β-Ga_2O_3 films grown by pulsed laser deposition on c-plane sapphire. It is clearly seen that the thermal conductivity of β-Ga_2O_3 thin films strongly depends on film thickness up to several micrometers, which can be mainly attributed to strong size effects associated with phonon-boundary scattering.

Fig. 2 also examines the β-Ga_2O_3 thermal conductivity dependence on Sn doping concentration, N_{Sn}, and displays that the model predictions with N_{Sn} ranging from 0 (i.e., no doping) to 1 $\times 10^{21}$ cm^{-3} are consistent with the literature data [34,36,41,51]

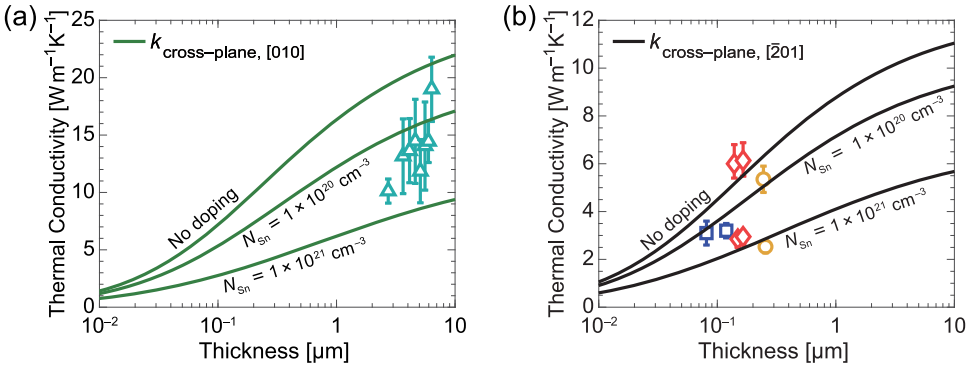

Fig. 2. Cross-plane thermal conductivity of (a) (010)- and (b) ($\bar{2}$01)-oriented β-Ga_2O_3 thin films as a function of film thickness at room temperature. The predictions of our model [Eqs. (1) and (4)] with varying Sn doping concentration N_{Sn} (green and black solid lines, respectively) are compared with the literature data (symbols). Legend: (a) triangles [41]; (b) red diamonds [34], blue squares [36], and yellow circles [51].

for both [010] and [$\bar{2}$01] directions. Although our modeling approach focuses on dopant scattering as well as isotope scattering, our approach can be extended to take into account phonon scattering on other imperfections, such as dislocations, stacking faults and grain boundaries, by employing appropriate expressions. We also compare the predictions of our cross-plane thermal conductivity model with those of other theoretical models based on the Debye-Callaway formalism [9,51] for both [010] and [$\bar{2}$01] directions. This comparison is provided in Fig. S3 of Supplementary Material, which shows that our model predictions are in reasonable agreement with those of the Debye-Callaway models. We note that, however, the exact shape of the thin-film thermal conductivity versus thickness curve slightly differs between the models, which can be attributed to the fact that each model is based on different assumptions regarding phonon dispersion as well as on different formulas to treat phonon-boundary scattering.

As depicted in Fig. S1 of Supplementary Material, our model calculations exhibit that the thermal conductivity of ($\bar{2}$01)-oriented β-Ga_2O_3 in both bulk and thin film forms shows no significant dependence on Sn doping concentrations up to approximately 1×10^{19} cm^{-3}. This agrees with a prior estimation of the threshold Sn concentration of 1×10^{19} cm^{-3}, above which the thermal conductivity begins to decrease with doping, for ($\bar{2}$01)-oriented β-Ga_2O_3 thin films [51]. This is also in agreement with previous experimental observations that the Sn doping does not significantly reduce the thermal conductivity of β-Ga_2O_3 crystals with doping levels below 1×10^{19} cm^{-3} [37,58]. Given that typical doping levels in β-Ga_2O_3 devices are less than 1×10^{19} cm^{-3} (except the level at source and drain contacts) [1,7,14,15,32,52], the effect of doping on the thermal conductivity of β-Ga_2O_3 can be neglected in our finite element device thermal model. We thus assume $N_{Sn} = 0$ (i.e., no doping) and do not consider any effects associated with doping. Since the purpose of this work is to evaluate the limits of the heat dissipation performance of sub-micrometer β-Ga_2O_3 devices on diamond, we also assume that the β-Ga_2O_3 layer approaches near crystalline perfection and thereby do not take into account any effects associated with external defects. We do consider, however, phonon scattering on isotopes; the isotope scattering strength Γ of 2.76×10^{-4} yields the cross-plane thermal conductivities of 4.5, 8.8, and 11.0 W m^{-1} K^{-1} at the ($\bar{2}$01) β-Ga_2O_3 film thicknesses of 0.1, 1, and 10 μm, respectively.

Figs. 3(a) and (b) show the cross-plane and in-plane thermal conductivity of β-Ga_2O_3 thin films, respectively, as a function of film thickness at room temperature, predicted by our model [Eqs. (1) and (4) and Eqs. (1) and (2) for cross-plane and in-plane heat flow, respectively]. To generate the results shown in Figs. 3(a) and (b), each crystallographic direction of β-Ga_2O_3 is assumed to be oriented along the cross-plane and in-plane directions of the film, respectively. Note again that we do not consider any effects associated with doping and external defects, while we consider the isotope scattering to treat Γ. As illustrated in Figs. 3(a) and (b), the thermal conductivity along the [010] direction is higher than those along the other three directions, consistent with the trend observed previously for bulk β-Ga_2O_3 [8]. Figs. 3(a) and (b) also clearly show that the thermal conductivity of β-Ga_2O_3 thin films with sub-micrometer thicknesses is significantly reduced for both cross-plane and in-plane directions, as compared to that of their bulk counterparts, suggesting that such size effects should be considered in the device thermal simulation. The results of our thermal conductivity calculations, as displayed in Fig. 3 as well as in Figs. S4 and S5 of Supplementary Material, are used as inputs to our finite element device thermal model.

Fig. 4 plots the maximum device temperature (T_{max}) as a function of β-Ga_2O_3 layer thickness (d), ranging from 0.1 to 10 μm, for seven possible crystallographic orientations of the β-Ga_2O_3 layer—from Case 1 to Case 7, as described in Section 2.1—in our single-gate Ga_2O_3-on-diamond device thermal model at a dissipated power density of 1.8 W mm^{-1}. As a Ga_2O_3/diamond TBC, we consider 20 and 180 MW m^{-2} K^{-1} (as discussed in Section 2.2), which are close to the lower and upper ends of a range of experimental values reported in the literature (from 17 to 179 MW m^{-2} K^{-1} [33,35]), respectively. A general trend of decreasing T_{max} with decreasing d is observed for all the cases considered here, predominantly owing to the high thermal resistance of the Ga_2O_3 layer associated with its inherent low thermal conductivity. For example, when the TBC is 180 MW m^{-2} K^{-1}, reducing d from 10 to 0.1 μm results in approximately 141 and 282 °C (70 and 79%) reductions in T_{max} for Cases 1 and 4, respectively. When the TBC is set to be 20 MW m^{-2} K^{-1}, the corresponding reductions are approximately 70 and 208 °C (34 and 57%) for Cases 1 and 4, respectively. Comparing the 0.1 μm and 1 μm Ga_2O_3 devices, particularly when the TBC is 180 MW m^{-2} K^{-1}, the values of T_{max} in the 0.1 μm device are approximately 53 and 108 °C (47 and 59%) lower than those in the 1 μm devices for Cases 1 and 4, respectively. These observations highlight that the key to maximizing the device-level cooling performance of β-Ga_2O_3 devices is to minimize the thermal resistance between the near-surface active device region (where heat generation occurs) and the high-thermal-conductivity substrate. In other words, to enhance the heat dissipation performance of β-Ga_2O_3 devices, it is important to locate the high-thermal-conductivity substrate as close as possible to the active device region.

We find that T_{max} becomes lower for Cases 1 and 2, where the [010] direction with the highest thermal conductivity is oriented along the cross-plane direction, as compared to other cases. It is also seen that Case 5 (Case 6), where the [001] direction is placed

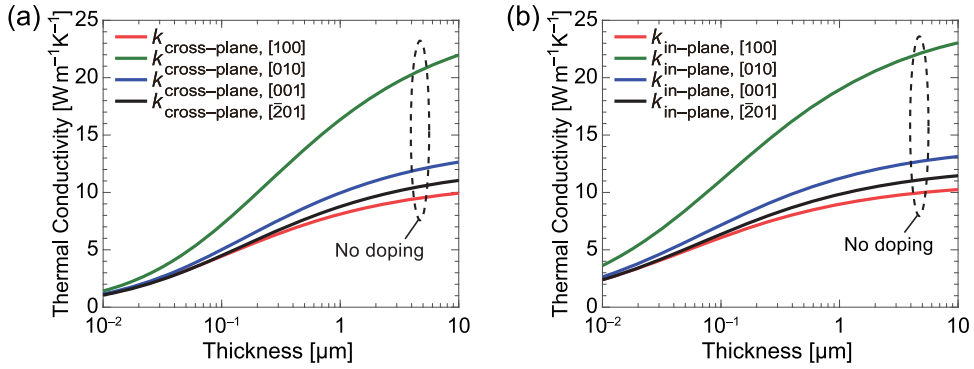

Fig. 3. (a) Cross-plane and (b) in-plane thermal conductivity of β-Ga_2O_3 thin films versus film thickness at room temperature, predicted by our model [Eqs. (1) and (4) and Eqs. (1) and (2) for cross-plane and in-plane heat flow, respectively]. Each crystallographic direction of β-Ga_2O_3 is assumed to be oriented along the (a) cross-plane and (b) in-plane directions of the film. To generate the results in (a) and (b), our analytical model assumes $N_{Sn} = 0$ (i.e., no doping) and considers phonon scattering on isotopes, yielding $\Gamma = 2.76 \times 10^{-4}$.

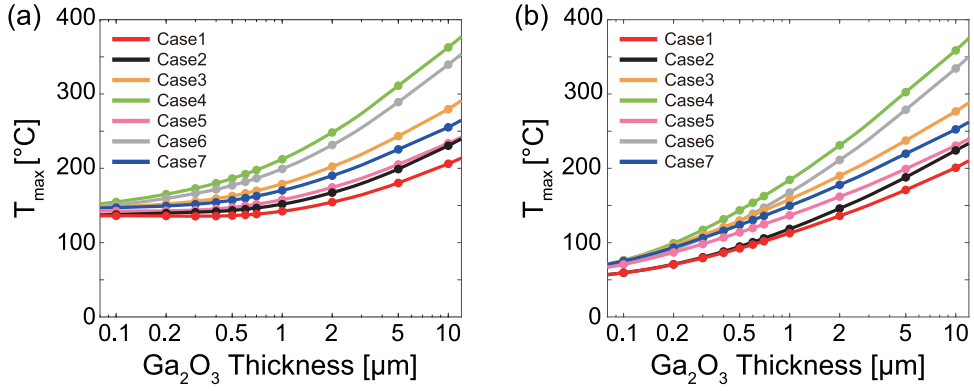

Fig. 4. Variation of maximum device temperature (T_{max}) with respect to β-Ga_2O_3 layer thickness for seven possible crystallographic orientations of the β-Ga_2O_3 layer—from Case 1 to Case 7—in our single-gate Ga_2O_3-on-diamond device thermal model, where Ga_2O_3/diamond TBCs are assumed to be (a) 20 and (b) 180 MW m^{-2} K^{-1} and a dissipated power density is assumed to be 1.8 W mm^{-1}.

in parallel to the cross-plane direction, has lower T_{max} than Case 3 (Case 4) with [100] in parallel to the cross-plane direction. T_{max} for Case 7, where the [$\bar{2}$01] direction is placed along the cross-plane direction and the [010] direction is assumed along both the heater length and width directions, projects to be between those for Cases 5 and 6, while it projects to be lower than those for Cases 3 and 4. Given that $k_{[010]} > k_{[001]} > k_{[\bar{2}01]} > k_{[100]}$, these observations indicate that it is beneficial to align the higher k direction along the cross-plane direction for the purpose of facilitating efficient heat transfer from the active device region to the high-thermal-conductivity substrate.

The optimal cooling performance of β-Ga_2O_3 devices is found to be achieved with Case 1, where the [010] direction is along the cross-plane direction and the [001] and [100] directions are along the heater length and width, respectively. Case 2, where [100] and [001] are the respective directions along the heater length and width with [010] along the cross-plane direction, yields the second lowest T_{max}. Given that $k_{[001]} > k_{[100]}$, this suggests that the higher k along the heater length direction is more effective at dissipating heat laterally within the β-Ga_2O_3 layer than the higher k along the heater width direction. A comparison between Cases 3 and 4, as well as between Cases 5 and 6 also reveals that the configuration with [010] along the heater length direction exhibits improved heat dissipation performance than that with [010] along the heater width direction. It is also of note that even with its lower cross-plane thermal conductivity, T_{max} of Case 5 is comparable to that of Case 2, particularly when the TBC is low (see Fig. 4(a)). This can be ascribed to enhanced lateral spreading of heat in the Ga_2O_3 layer for Case 5 (with [010] as the heater length direction) as compared to Case 2 (with [100] as the heater length direction). Comparing Cases 5 and 7, Case 7 has higher T_{max} than Case 5 primarily due to its lower cross-plane thermal conductivity. However, despite its lower cross-plane thermal conductivity, Case 7 has lower T_{max} than Case 6, which can be attributed to the effect associated with [010] and [100] being aligned along the heater length direction for Cases 7 and 6, respectively. All these findings confirm that more effective lateral heat dissipation channel is oriented along the gate length rather than the gate width in β-Ga_2O_3 devices with highly anisotropic k.

We also note that the difference in T_{max} between Case 1 and Case 4 (which yields the lowest and highest T_{max}, respectively, across all thicknesses considered here) decreases as the Ga_2O_3 layer thickness decreases. This difference is approximately 157, 70, and 19 °C (158, 72, and 17 °C) at the Ga_2O_3 thicknesses of 10, 1, and 0.1 μm, respectively, when the TBC is 20 MW m^{-2} K^{-1} (180 MW m^{-2} K^{-1}). This implies that the impact of the crystallographic orientation of the Ga_2O_3 layer on T_{max} becomes smaller as the Ga_2O_3 layer becomes thinner, which can be ascribed to the decreasing contribution of the Ga_2O_3 layer to T_{max} with decreasing Ga_2O_3 thickness (as evident from Fig. 5). This also implies that approximately 43, 33, and 12% (44, 39, and 22%) reductions in T_{max} can be attained by switching from Case 4 to Case 1 at the Ga_2O_3 thicknesses of 10, 1, and 0.1 μm, respectively, when the TBC is 20 MW m^{-2} K^{-1} (180 MW m^{-2} K^{-1}).

To gain further insight into the impact of the Ga_2O_3 layer thickness on T_{max}, we decompose the contribution of each layer of the Ga_2O_3-on-diamond structure to the device thermal resistance—which is defined as the maximum temperature rise of the device

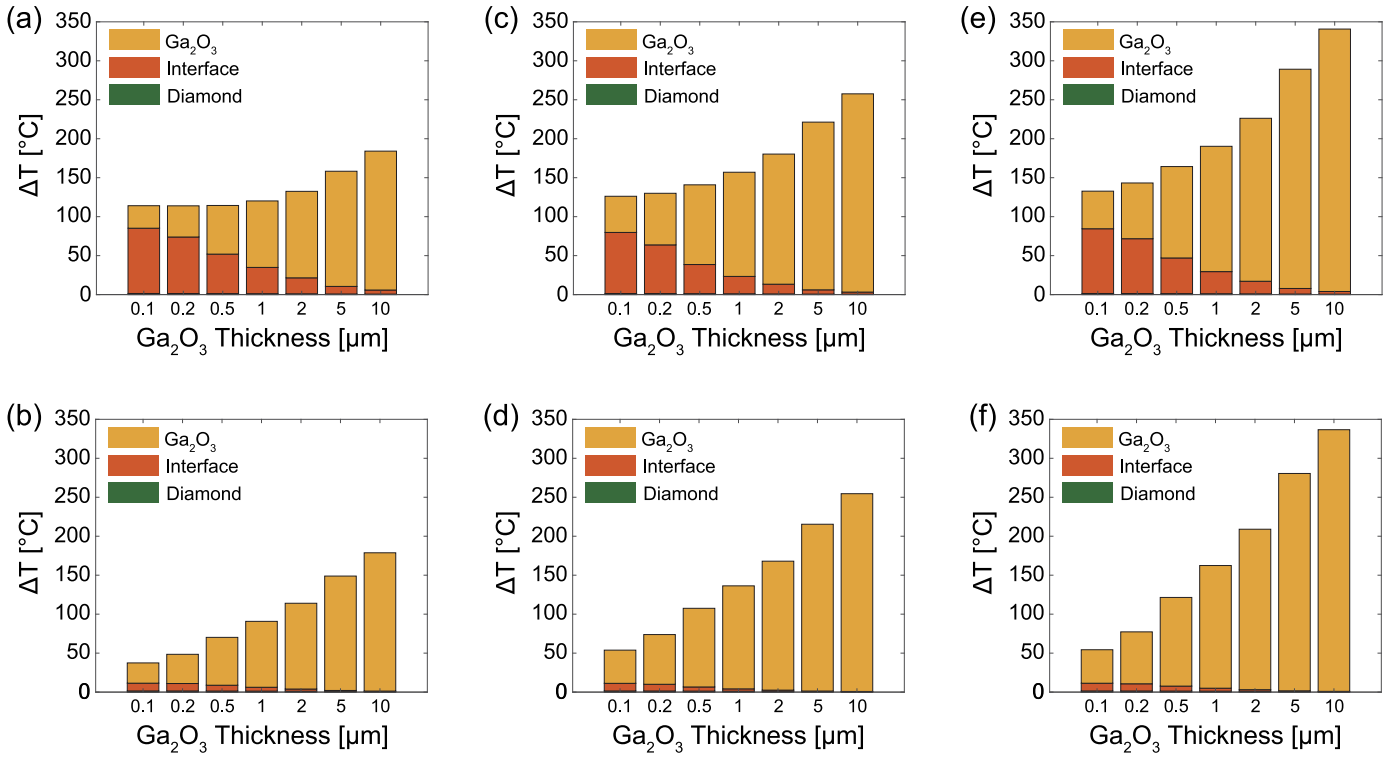

Fig. 5. Maximum device temperature rise, with the reference of a bottom boundary temperature of 22 °C, as a function of Ga_2O_3 layer thickness for (a,b) Case 1, (c,d) Case 3, and (e,f) Case 4. Relative temperature rises across each layer beneath the peak temperature position of our single-gate Ga_2O_3-on-diamond device model are evaluated at 1.8 W mm^{-1} power dissipation. The Ga_2O_3/diamond TBC assumed in (a), (c), and (e) is 20 MW m^{-2} K^{-1}, while that in (b), (d), and (f) is 180 MW m^{-2} K^{-1}.

(relative to a bottom boundary temperature of 22 °C) divided by its dissipated power. Fig. 5 plots relative temperature rises across the Ga_2O_3 layer, Ga_2O_3/diamond interface, and diamond substrate for Cases 1, 3, and 4, obtained from the vertical temperature-depth profiles beneath the peak temperature position of the single-gate Ga_2O_3-on-diamond device model. Dividing their respective temperature rises by the dissipated power density (1.8 W mm^{-1}), we quantify their respective contributions to the device thermal resistance. As clearly seen in Fig. 5, the thermal resistance of the Ga_2O_3 layer ($R_{Ga_2O_3}$) monotonically decreases with decreasing Ga_2O_3 layer thickness for all three cases. This trend is, as discussed above, strongly associated with the inherently low thermal conductivity of the Ga_2O_3 layer. For example, the values of $R_{Ga_2O_3}$ for Case 1 are around 99, 47, and 16 mm °C W^{-1} (99, 47, and 14 mm °C W^{-1}) at the Ga_2O_3 thicknesses of 10, 1, and 0.1 μm, respectively, when the Ga_2O_3/diamond TBC is 20 MW m^{-2} K^{-1} (180 MW m^{-2} K^{-1}). The values of $R_{Ga_2O_3}$ for Case 3 (Case 4) are approximately 141, 74, and 26 mm °C W^{-1} (187, 89, and 27 mm °C W^{-1}) at the Ga_2O_3 thicknesses of 10, 1, and 0.1 μm, respectively, for the TBC of 20 MW m^{-2} K^{-1}, while for the TBC of 180 MW m^{-2} K^{-1} those for Case 3 (Case 4) are approximately 141, 73, and 24 mm °C W^{-1} (187, 87, and 24 mm °C W^{-1}) at the Ga_2O_3 thicknesses of 10, 1, and 0.1 μm, respectively. The higher $R_{Ga_2O_3}$ values for Case 4 than those for Case 3 are mainly owing to the lower k direction (i.e., [001]) aligned along the heater length for Case 4, as compared to the higher k direction (i.e., [010]) along the heater length for Case 3.

Due to its intrinsic high thermal resistance, the Ga_2O_3 layer is a dominant contributor to the device thermal resistance, particularly when the TBC is high (the TBR is low); see Figs. 5(b), (d) and (f). Taking Case 1 as an example, when the TBC is 180 MW m^{-2} K^{-1}, the Ga_2O_3 layer accounts for approximately 99, 93, and 69% of the device thermal resistance at its thicknesses of 10, 1, and 0.1 μm, respectively. For Case 4, this contribution is about >99, 97, and 79% at the Ga_2O_3 thicknesses of 10, 1, and 0.1 μm, respectively. When the TBC is low (i.e., 20 MW m^{-2} K^{-1}), around 97, 71, and 25% of the device thermal resistance of Case 1 are attributable to the Ga_2O_3 layer of thicknesses 10, 1, and 0.1 μm, respectively. For Case 4, this contribution is about 99, 84, and 36% at the Ga_2O_3 thicknesses of 10, 1, and 0.1 μm, respectively.

Another point to note in Fig. 5 is that the Ga_2O_3/diamond interface contributes greater to the device thermal resistance as the Ga_2O_3 layer becomes thinner. The lower the TBC (the higher the TBR), the more pronounced this trend is; compare Figs. 5(a), (c), and (e) with Figs. 5(b), (d), and (f). For instance, the interface accounts for around 3, 28 and 73% of the device thermal resistance for Case 1 at the Ga_2O_3 thicknesses of 10, 1, and 0.1 μm, respectively, for the TBC of 20 MW m^{-2} K^{-1}, while for the TBC of 180 MW m^{-2} K^{-1} the corresponding contributions of the interface are around <1, 5 and 27% at the Ga_2O_3 thicknesses of 10, 1, and 0.1 μm, respectively. As the Ga_2O_3 layer becomes thinner, a decreasing fraction of the heat generated in the active device region is diffused laterally within the Ga_2O_3 layer, owing to i) the smaller volume and ii) the reduced thermal conductivity associated with the size effect. This means that an increasing fraction of the heat is dissipated at the interface, leading to its increasing contribution to the device thermal resistance. This also explains an increase in the substrate thermal resistance with decreasing Ga_2O_3 layer thickness (i.e., more heat dissipation occurs in the substrate for thinner Ga_2O_3 layers), although the substrate thermal resistances remain to be very low (< 1.5 mm °C W^{-1}) for all the Ga_2O_3 thicknesses (due to the intrinsic high thermal conductivity of diamond).

We then compare the heat dissipation performance of single-gate Ga_2O_3 devices on diamond and SiC. Fig. 6 shows T_{max} versus Ga_2O_3 layer thickness for both device models at 1.8 W mm^{-1} power density. Taken from experimental values obtained from the

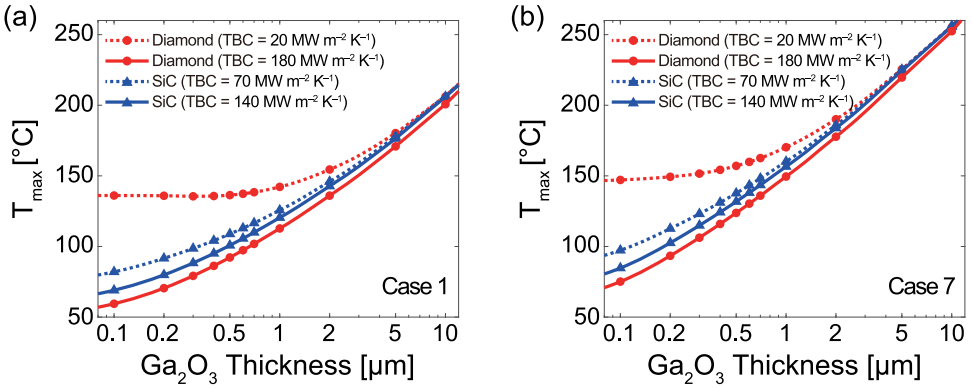

Fig. 6. Maximum device temperature (T_{max}) as a function of Ga_2O_3 layer thickness for single-gate Ga_2O_3 devices on diamond and SiC at a power density of 1.8 W mm^{-1}. Circles and triangles represent the Ga_2O_3-on-diamond and Ga_2O_3-on-SiC devices, respectively. Solid and dotted lines correspond to the upper and lower bounds (i.e., the best-case and worst-case values) of a range of experimental TBC values reported in the literature, respectively. This range is 20–180 MW m^{-2} K^{-1} for the Ga_2O_3-on-diamond and 70–140 MW m^{-2} K^{-1} for the Ga_2O_3-on-SiC. The crystallographic orientation of the Ga_2O_3 layer is assumed to be that of (a) Case 1 and (b) Case 7.

literature, as detailed in Section 2.2, 20–180 and 70–140 MW m^{-2} K^{-1} are assumed as the Ga_2O_3/diamond and Ga_2O_3/SiC TBCs, respectively. The lower and upper bounds of each range represent the worst-case and best-case values of the corresponding TBC, respectively. To make a fair comparison, the crystallographic orientation of the Ga_2O_3 layer is assumed to be the same for both device models. We first consider Case 1, which yields the device's best cooling performance as compared to others. As illustrated by red and blue solid lines in Fig. 6(a), assuming their respective best-case TBC values, the Ga_2O_3-on-diamond exhibits lower T_{max} values than the Ga_2O_3-on-SiC across all the Ga_2O_3 layer thicknesses studied here. This shows that the optimum heat dissipation performance of Ga_2O_3 devices on diamond exceeds that of Ga_2O_3 devices on SiC. Assuming their respective worst-case TBC values, however, T_{max} for the Ga_2O_3-on-diamond is higher than that for the Ga_2O_3-on-SiC (see red and blue dotted lines in Fig. 6(a)). A comparison between the Ga_2O_3-on-diamond and Ga_2O_3-on-SiC devices for Case 7 is also provided in Fig. 6(b). Although the modeled T_{max} values of Case 7 are higher than those of Case 1, mainly due to its lower cross-plane thermal conductivity, similar trends are observed as in Case 1.

It is worth noting that the benefit of using the diamond substrate becomes more noticeable as the Ga_2O_3 layer becomes thinner. As explained above, as the Ga_2O_3 layer thickness decreases, an increasing fraction of the heat is dissipated in the substrate, as well as at the interface, and thereby the substrate increasingly contributes to T_{max}. Taking Case 1 as an example, as quantified from Fig. 6(a), around 14, 8, 6, and 2% reductions in T_{max} can be obtained at the Ga_2O_3 thicknesses of 0.1, 0.5, 1, and 10 μm, respectively, by switching from the SiC substrate to diamond under 1.8 W mm^{-1} power density. Also, as depicted later in Fig. 7(a), this improvement in heat dissipation becomes more pronounced with increasing power density. Taking the 0.1 μm Ga_2O_3 device on diamond as an example, approximately 18 and 21% reductions in T_{max} can be achieved at 4 and 10 W mm^{-1}, respectively, as compared to that on SiC. This indicates that the integration with diamond can be an effective approach to improve heat dissipation particularly for sub-1 μm Ga_2O_3 devices and also for higher output power applications.

As a next step, we evaluate the power handling capability limits of Ga_2O_3 devices on diamond—i.e., the maximum possible power density (P_{max}) that these devices can reach under a safe junction temperature limit of 200 °C (as previously established by Refs. [15,16]). Fig. 7 shows the modeled T_{max} as a function of dissipated power density for the Ga_2O_3 devices on both diamond and SiC, where the Ga_2O_3 layer thicknesses range from 0.1 to 10 μm. In order to explore the upper limits of P_{max} for both Ga_2O_3-on-diamond and Ga_2O_3-on-SiC devices, their respective best-case scenarios are considered, assuming their respective best-case TBC values as well as Case 1 as the crystallographic orientation of the Ga_2O_3 layer. We first observe that the device thermal resistance—which is defined as the ratio of the device peak temperature rise to the dissipated power density—decreases with decreasing Ga_2O_3 layer thickness, as can be deduced from the slopes of the T_{max} versus P plot in Fig. 7. Consistent with findings in Figs. 4–6, this trend can be again attributed to the low thermal conductivity of the Ga_2O_3 layer. It is also observed in Fig. 7 that the device thermal resistance gradually increases (i.e., the slope gradually increases) with increasing power density, due to the $1/T$ temperature dependence of the thermal conductivity of Ga_2O_3 and substrate materials.

Considering power density up to 1.8 W mm^{-1}, the device thermal resistances are estimated to be ~96.3, 80.6, 49.7, 38.6, and 20.7 mm °C W^{-1} at the Ga_2O_3 thicknesses of 10, 5, 1, 0.5, and 0.1 μm, respectively, for the Ga_2O_3-on-diamond. It is notable that the thermal resistances of the 0.1 and 0.5 μm devices on diamond can be ~3–5× lower than that of the 10 μm device on diamond. These resistances for the Ga_2O_3-on-SiC are found to be higher than those for the Ga_2O_3-on-diamond, with ~98.6, 83.5, 53.8, 43.2, and 26.0 mm °C W^{-1} estimated for the Ga_2O_3 thicknesses of 10, 5, 1, 0.5, and 0.1 μm, respectively. This translates into ~2.3, 3.5, 7.6, 10.7, and 20.4% reductions in the device thermal resistance at the Ga_2O_3 thicknesses of 10, 5, 1, 0.5, and 0.1 μm, respectively, when the SiC substrate is replaced by diamond.

We proceed to find P_{max} for each device configuration with the target junction temperature of 200 °C. For Ga_2O_3 devices on diamond, P_{max} is found to be 1.80, 2.07, 3.15, 4.00, and 7.67 W mm^{-1} at the Ga_2O_3 thicknesses of 10, 5, 1, 0.5, and 0.1 μm, respectively. It should be noted that P_{max} of the 0.1 μm device is ~4.3 times higher than that of the 10 μm device. Lower P_{max} values of 1.76, 2.01, 2.94, 3.62, and 6.17 W mm^{-1} are estimated for Ga_2O_3 devices on SiC with the Ga_2O_3 thicknesses of 10, 5, 1, 0.5, and 0.1 μm, respectively. This indicates ~7, 11, and 24% increases in P_{max} with the SiC substrate replaced by diamond for the 1, 0.5, and 0.1 μm devices, respectively. In other words, P_{max} of sub-1 μm Ga_2O_3 devices on diamond can be up to ~24% higher than that of Ga_2O_3-on-SiC at the same Ga_2O_3 layer thickness. For the 5 and 10 μm devices, the corresponding increases in P_{max} are less than 3%. These observations again demonstrate the utility of employing the diamond substrate, particularly for sub-1 μm Ga_2O_3 devices, as an effective bottom-side passive cooling solution. Thicker Ga_2O_3 devices ($d >$ 1 μm) on diamond and SiC may have similar performance in heat dissipation, consistent with past observations [16,39].

Our ultimate aim is to assess the theoretical maximum power density for sub-1 μm Ga_2O_3 devices on diamond, which sets the

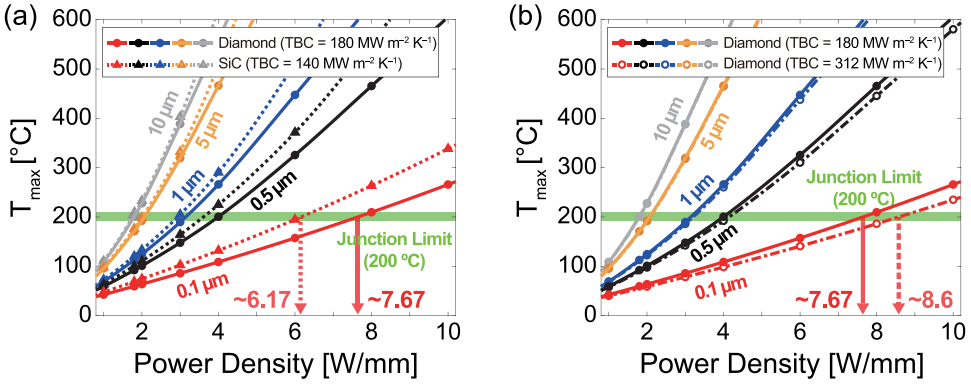

Fig. 7. Maximum device temperature (T_{max}) as a function of dissipated power density for single-gate Ga_2O_3 devices, where the thickness of the Ga_2O_3 layer ranges from 0.1 to 10 µm and its crystallographic orientation is assumed to be that of Case 1. With 200 °C assumed as a safe junction temperature limit (as previously established by Refs. [15,16]), the maximum possible power density (P_{max}) is obtained for the Ga_2O_3 devices on both diamond and SiC. (a) The Ga_2O_3 devices on diamond (filled circles) are compared with those on SiC (filled triangles), assuming their respective best-case TBC values (i.e., 180 and 140 MW m^{-2} K^{-1}, respectively). (b) The Ga_2O_3-on-diamond devices with the best-case TBC of 180 MW m^{-2} K^{-1} (filled circles) are compared to those with a theoretical upper limit of 312 MW m^{-2} K^{-1} for the TBC (open circles).

fundamental upper limit of P_{max} for these devices. We attempt to evaluate this limit by considering a theoretical upper limit of the TBC for a perfect β-Ga_2O_3/diamond interface, as well as Case 1 as the crystallographic orientation of the Ga_2O_3 layer. The former is adapted from Ref. [33], where the TBC between β-Ga_2O_3 and diamond was predicted to be 312 MW m^{-2} K^{-1} by utilizing a Landauer approach with phonon transmission probability estimated from the diffuse mismatch model (DMM) [59]. The DMM is commonly used for describing phonon-dominated interfacial thermal transport and assumes that all phonons are diffusely and elastically scattered at the interface [59]. The DMM essentially assumes that interfacial phonon transport is dictated by the inherent mismatch in the phonon density of states between two contacting materials, not by any extrinsic effects such as near-interfacial defects [10,21]. This model thereby sets a fundamental upper limit for the TBC. With these considerations, P_{max} for the 0.1 µm Ga_2O_3 device on diamond further increases up to ~8.6 W mm^{-1}, which translates into an ~12% increase in P_{max} when compared to that (7.67 W mm^{-1}) for the same device with the best-case experimental TBC being considered. This increase becomes increasingly negligible as the Ga_2O_3 layer becomes thicker, as seen in Fig. 7(b), due to the diminishing impact of the interface with increasing Ga_2O_3 thickness (as also evident in Fig. 5). For example, this increase is ~4 and 2% for the 0.5 and 1 µm devices, respectively, and no increase is observed for the thicker devices (d > 1 µm). Section S2(d) of Supplementary Material provides further insight into the impact of the TBC on the device power handling capability.

It should be noted that the fundamental upper limit of P_{max} for sub-1 µm Ga_2O_3 devices on diamond (up to 8.6 W mm^{-1}) is comparable to a range of P_{max} from 7.3 to 16 W mm^{-1} simulated previously with an augmented device-level thermal management scheme—i.e., a double-side cooling (i.e., both top-side and bottom-side cooling) design combined with an active region heat spreader, as previously presented as a limiting case for the maximum thermal performance of Ga_2O_3 lateral transistors [16]. This suggests that the integration with diamond can fundamentally enhance the device-level cooling performance of Ga_2O_3 electronics, sub-1 µm devices in particular, without requiring additional cooling components and complexity associated with costly augmented thermal management designs that may negatively impact the system size, weight and power (SWaP).

Considerable efforts are being made to realize a scalable β-Ga_2O_3/diamond heterostructure for energy-efficient, high-performance power semiconductor devices. For example, one recent effort [32] fabricated devices based on mechanically exfoliated β-Ga_2O_3 nanomembranes (50–150 nm) that were transferred on single crystal diamond substrates via van der Waals bonding, and achieved a record high drain current of 980 mA mm^{-1}. However, these exfoliated devices have limited scaling capability and cannot be supported by wafer-scale manufacturing. Another recent effort [60] demonstrated the direct bonding of β-Ga_2O_3 wafers and single-crystal diamond wafers at a relatively low temperature (250 °C), but the β-Ga_2O_3 wafers were not thinned down to thin-film forms. In addition to these bonding approaches, direct growth of β-Ga_2O_3 thin films on single crystal diamond has been pursued [35,61]. One example is nanocrystalline β-Ga_2O_3 thin films (28–115 nm) grown by ALD on single crystal diamond substrates [35]. These films, however, are not of device-grade quality with a low thermal conductivity of ~1.5 W m^{-1} K^{-1}, predominantly due to their small grain sizes (~10 nm) and the potential existence of phase impurities. All of these suggest that a scalable approach for heterogeneously integrating high-quality sub-micrometer β-Ga_2O_3 films onto diamond substrates is still lacking, which is essential for the commercialization of sub-micrometer β-Ga_2O_3 devices on diamond. Such a scalable heterointegration approach must not adversely affect the electrical performance of devices. It should be also noted that any implementation of β-Ga_2O_3-diamond heterointegration must manage the strain induced by the mismatch in lattice constants and thermal expansion coefficients between β-Ga_2O_3 and diamond, such that the heterointerface stays intact under high temperature conditions associated with film growth or subsequent device-processing steps.

Finally, a multi-finger device model (20 fingers and 10–40 µm gate pitch (s)) is considered to evaluate the potential of sub-1 µm Ga_2O_3 devices on diamond for higher output power applications. Fig. 8 shows lateral surface temperature profiles of the symmetric quarter of the multi-finger Ga_2O_3-on-diamond device model with the gate pitches of 10 and 40 µm and the Ga_2O_3/diamond TBCs of 20 and 180 MW m^{-2} K^{-1} at 1.8 W mm^{-1} power density. The maximum device temperature occurs at the central finger, the position of which is indicated by the leftmost temperature peak. When the Ga_2O_3 layer thickness is 10 µm (Fig. 8(a)), a thermal crosstalk between individual fingers is evident on the 10 µm-pitch multi-finger device, and the maximum device temperatures are increased by ~55 and 45 °C, as compared to the single-gate device, for the TBCs of 20 and 180 MW m^{-2} K^{-1}, respectively. The corresponding increases with the 40 µm gate pitch are 1.8 and 1.7 °C for the TBCs of 20 and 180 MW m^{-2} K^{-1}, respectively, clearly showing that the thermal crosstalk effect becomes less significant with increasing gate pitch. When the Ga_2O_3 layer is 1 µm (Fig. 8(b)), this increase for the 10 µm (40 µm)-pitch device is reduced to 4.2 °C (1.2 °C) for both TBC values, while when the Ga_2O_3 layer is 0.1 µm

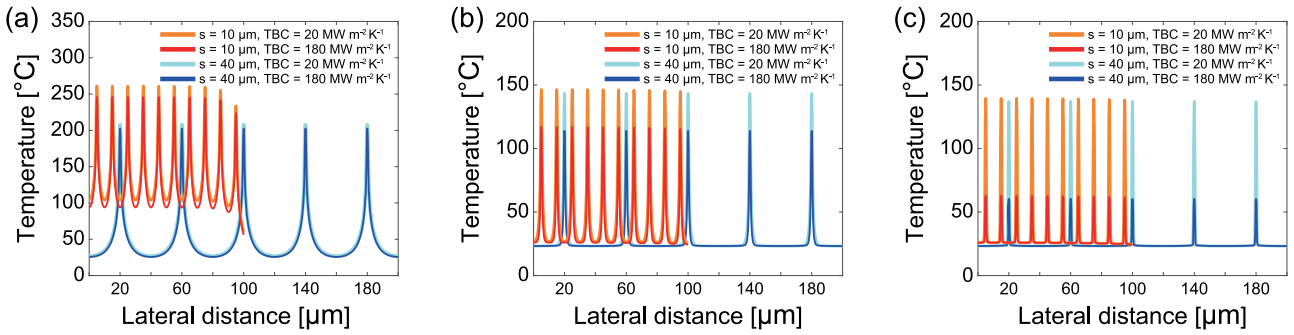

Fig. 8. Lateral surface temperature profiles of the symmetric quarter of a multi-finger Ga_2O_3-on-diamond device model (20 fingers and 10–40 μm gate pitch (s)) with Ga_2O_3/diamond TBCs of 20 and 180 MW m^{-2} K^{-1} at 1.8 W mm^{-1} power density. The maximum device temperature occurs at the central finger, the position of which is indicated by the leftmost temperature peak. The crystallographic orientation of the Ga_2O_3 layer is taken to be that of Case 1 and its thickness is assumed to be (a) 10 μm, (b) 1 μm, and (c) 0.1 μm.

(Fig. 8(c)), that for the 10 μm (40 μm)-pitch device is further reduced to 3.3 °C (1.0 °C) for both TBC values. These observations imply that the thermal crosstalk effect becomes almost negligible as the Ga_2O_3 layer thickness is reduced to below 1 μm, predominantly owing to the dominant impact of the diamond substrate on the heat dissipation of sub-1 μm Ga_2O_3 devices on diamond. These findings also clearly demonstrate the potential benefits of sub-1 μm multi-finger Ga_2O_3 transistors on diamond for higher output power applications.

4. Conclusions

This work assesses via finite element simulations the fundamental limits to device-level conduction cooling of sub-1 μm β-Ga_2O_3 devices integrated with diamond. A semi-classical phonon transport model is employed here to systematically calculate the thickness-dependent thermal conductivity of the β-Ga_2O_3 layers with different crystallographic orientations for both cross-plane and in-plane directions. We find that the optimal cooling performance of β-Ga_2O_3 devices is achieved when the [010] direction with the highest thermal conductivity is oriented along the cross-plane direction. It is also found that aligning the higher thermal conductivity direction along the gate length is more effective at dissipating heat laterally than along the gate width in these devices. Considering the optimal device orientation as well as best-case experimental Ga_2O_3/diamond TBC, our simulation results exhibit that sub-1 μm Ga_2O_3 devices on diamond, particularly the 0.1 μm device, can handle a maximum power density as high as 7.7 W mm^{-1} with a junction temperature limit of 200 °C, which is ~4.3 times higher than that of the 10 μm device. It is also simulated that the maximum power density of sub-1 μm Ga_2O_3 devices on diamond can be up to ~24% higher than that of Ga_2O_3-on-SiC at the same Ga_2O_3 layer thickness. As the Ga_2O_3/diamond TBC approaches the upper limit predicted by the DMM, the power handling capability of these devices can be increased up to 8.6 W mm^{-1}, which is comparable to those reported previously for costly augmented thermal management designs (e.g., double-side cooling with additional active region heat spreader). The findings of this work suggest that the integration with diamond, as a bottom-side passive cooling method, can fundamentally increase the power handling capability of sub-1 μm Ga_2O_3 devices and potentially reduce system-level cooling costs and packaging challenges.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

CRediT authorship contribution statement

Taeyeon Kim: Methodology, Software, Validation, Formal analysis, Investigation, Visualization. **Sung Il Park:** Methodology, Software, Validation, Formal analysis, Investigation, Visualization. **Changhwan Song:** Methodology, Software, Investigation. **Hyoungsoon Lee:** Methodology, Investigation. **Jungwan Cho:** Conceptualization, Methodology, Formal analysis, Writing – original draft, Writing – review & editing, Supervision, Project administration, Funding acquisition.

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Supplementary materials

Supplementary material associated with this article can be found, in the online version, at doi:10.1016/j.ijheatmasstransfer.2022.122864.

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