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Fundamental limits for near-junction conduction cooling of high power GaN-on-diamond devices

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ABSTRACT

The integration of differing materials can enable breakthrough performance for semiconductor devices. One example is the integration of gallium nitride (GaN) and diamond to form GaN-on-diamond, which enables high-power GaN devices to achieve extreme power densities and, arguably, approaches fundamental limits for conduction cooling. Here, we examine the fundamental limits for near-junction phonon conduction cooling of GaN-on-diamond devices via finite element calculations of their lowest possible thermal resistance. A semi-classical transport theory for phonons interacting with interfaces and defects is used to calculate the in-plane thermal conductivity of a GaN epilayer and thereby accurately account for the thermal spreading resistance of the GaN layer. The device thermal resistance of a state-of-the-art GaN-on-diamond structure is predicted to be ~13.0 K mm W^{-1} for a 12 finger device with 30 μm gate-to-gate spacing and a power dissipation of 5 W mm^{-1}. For the same multifinger cell geometry and dissipated power, device thermal resistances as low as ~10.0 K mm W^{-1} may be possible with assuming anisotropic but homogeneous diamond, as well as the absence of phonon scattering by external defects in the GaN layer and interface.

1. Introduction

The thermal management of GaN high-electron-mobility transistors (HEMTs) has received much attention over the decades [1–3]. A high device heat flux and associated high junction temperature rise in these devices strongly limit device performance and reliability [4]. Among heat removal pathways from the heated electronic junction to the ambient air, heat removal very near the junction becomes increasingly important with increasing power density in these devices [1,2]. The so-called "near-junction" region in these devices consists of a GaN layer with a thickness up to a few micrometers on a substrate with a thickness up to a few hundred micrometers [1,2]. The choice of the substrate material strongly influences the near-junction heat spreading capability, and particular attention therefore has been paid to chemical-vapor-deposited (CVD) synthetic diamond, whose thermal conductivity is nearly a factor of 5 higher than that of SiC (which is presently used in the RF GaN industry) [1,2]. While integrating CVD diamond near the device junction, to form GaN-on-diamond, has shown some promise in enhancing the device power handling capability [5], a key question still remains to be answered: What are the fundamental limits to the near-junction conduction cooling of GaN-on-diamond devices? To address this question, we investigate the phonon conduction limits—i.e. the minimum (maximum) possible near-junction thermal resistances (conductances)—that may be achieved from a state-of-the-art GaN-on-diamond device structure.

2. Simulation method and details

The phonon heat conduction in multilayer GaN device structures is examined by performing calculations using a commercial FEM package. We determine the temperature field by solving the steady-state 2D heat diffusion equation for the multilayer stack with surface heating, and then assess the device thermal resistance (i.e., the maximum temperature rise in the device divided by its power dissipation) of both GaN-on-SiC and GaN-on-diamond structures. The device thermal resistance presented here can effectively account for the thermal resistances associated with the near-junction region, i.e., the thermal spreading resistances of the GaN layer and the substrate (SiC or diamond), as well as the thermal boundary resistance (TBR) at the interface between the GaN and the substrate.

Fig. 1 shows the simulation geometries for both GaN-on-SiC and GaN-on-diamond device structures, which reflect their respective contemporary best practice; 1.8 μm GaN layer on ~20–40 nm AlN transition layer on 95 μm SiC substrate and 1 μm GaN layer on ~5–30 nm SiN

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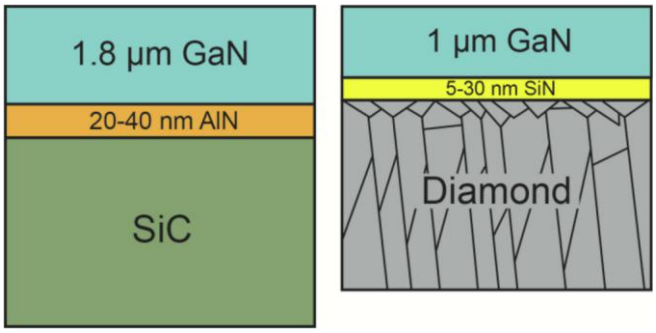

Fig. 1. Schematics of (a) GaN-on-SiC and (b) GaN-on-diamond device structures for thermal simulations.

interfacial layer on 95 μm diamond substrate [1,2,6–11]. Heteroepitaxy of GaN on SiC is generally achieved with a strained AlN transition layer, while a GaN-on-diamond fabrication technology involves the direct growth of CVD diamond on the backside of the GaN typically with a SiN barrier layer [1]. A region of heat generation in actual devices is modeled as a heater (either a single heater or an array of multiple heaters, which mimics single-gate and multi-finger devices, respectively) on the top surface [1,2,12]. The substrate is assumed to be heat-sinked ideally with a fixed temperature of 300 K at its bottom surface. All other surfaces of the structure, except the top and bottom surfaces, are assumed to be adiabatic.

The GaN-on-SiC thermal model assumes the best-case scenario for the thermal properties of the constituent layers and interfaces [6–8]. The thermal conductivity of the GaN layer (k_{GaN}) is taken from Ref. 6, where $167(T/300)^{-1.44}$ W m^{-1} K^{-1} was measured using time-domain thermoreflectance (TDTR) for a 1.6 μm GaN film on ~36 nm AlN on SiC. The thermal conductivity of the SiC substrate is assumed to be $330(T/300)^{-1.49}$ and $500(T/300)^{-1.49}$ W m^{-1} K^{-1} for the cross-plane and in-plane directions, respectively [6]. The TBR at the GaN/SiC interface is taken to be 5 m^2 K GW^{-1} [6–8], the lowest reported in the literature. The GaN/SiC TBR is an effective resistance that includes the volumetric AlN resistance and the two discrete GaN/AlN and AlN/SiC TBRs.

The GaN-on-diamond thermal model utilizes the best available literature for the TBR at the GaN/diamond interface and the thermal conductivity of the diamond substrate [8–11,13]. The GaN/diamond TBR is a lumped resistance, including contributions from i) a low-quality GaN region near the interface with the SiN layer, ii) two discrete SiN boundaries with the GaN and diamond, iii) the SiN layer, and iv) a near-interfacial diamond region (i.e., an initial, nanocrystalline nucleation/coalescence region adjacent to the growth interface with the GaN backside) [9]. Previous TDTR studies of GaN/SiN/diamond samples have reported the GaN/diamond TBR to be 17.4 and 9.5 m^2 K GW^{-1} for 22 and 5 nm SiN layers, respectively [8,9]. Other measurements using nanosecond transient thermoreflectance have reported ~12 and ~6.5 m^2 K GW^{-1} for 28 and 5 nm SiN layers, respectively [10,11]. Among these reported values, we take the lowest (6.5 m^2 K GW^{-1}) as the GaN/diamond TBR.

Thermal transport in diamond is inhomogeneous and anisotropic due to initial nucleation/coalescence of diamond grains and their subsequent columnar growth [13–15]. The temperature-dependent thermal conductivity of the diamond substrate in our thermal model is taken from a recent calculation [13], which utilized a semi-classical phonon thermal conductivity integral approach for two cases: i) inhomogeneous/anisotropic diamond and ii) anisotropic but homogeneous diamond. For the former, the 95 μm diamond substrate in the GaN/SiN/diamond structure was discretized into 5 sub-regions (0–1, 1–5, 5–15, 15–35, and 35–95 μm regions) and local cross-plane and in-plane thermal conductivities for each of these sub-regions were evaluated. For example, local cross-plane and in-plane thermal conductivities are ~318 and ~126 W m^{-1} K^{-1}, respectively, at room temperature for the first micrometer diamond. For the latter, cross-plane and in-plane thermal conductivities were averaged over the entire diamond thickness, yielding ~1737 and ~1335 W m^{-1} K^{-1}, respectively, at room temperature. As we discuss in Section 3, we consider both cases to evaluate the limits of thermal performance of GaN-on-diamond devices.

Many thermal conductivity data, although predominantly in the cross-plane direction, are available in the literature for GaN films of thickness similar to that used here in our thermal model [6,7,16–20]. Based on the existing literature, most prior thermal simulations for GaN devices have typically assumed $k_{GaN} = 160(T/300)^{-1.4}$ W m^{-1} K^{-1}, which typically corresponds to the cross-plane thermal conductivity of a few micrometers thick GaN film [21–23]. We note that, however, the in-plane thermal conductivity plays a more significant role than the cross-plane thermal conductivity particularly for GaN-on-diamond devices, where the TBR is relatively high as compared to that of GaN-on-SiC devices and the GaN layer thereby spreads heat laterally [9]. The in-plane thermal conductivity of the GaN layer therefore needs to be used when assessing the near-junction conduction cooling of GaN-on-diamond devices. A few recent studies have reported the in-plane thermal conductivity data [9,24], although all at room temperature. For example, 60 W m^{-1} K^{-1} was measured for a 0.15 μm GaN film using micro-Raman thermometry [24], and 101–117 W m^{-1} K^{-1} were measured for 0.58–0.85 μm GaN films on SiN/diamond using TDTR [9]. To our knowledge, the temperature-dependent data are currently unavailable.

To consider the temperature-dependent in-plane thermal conductivity of the 1 μm GaN layer in our GaN-on-diamond thermal model, we employ a semi-classical phonon thermal conductivity integral model [9,25–27] with a Sondheimer-type reduction function [9]. Our model considers an isotropic sinusoidal dispersion with three acoustic phonon branches lumped into a single, triply degenerate branch [9,26], as well as phonon scattering on point defects, boundaries, and other phonons. For simplicity, we consider only a vacancy as a type of point defect, because it is the strongest scatterer owing to the largest mass difference [6,9]. The model calculations with varying vacancy concentration n_v, along with literature data for the thermal conductivity of GaN films versus film thickness, at room temperature are provided in Fig. 2, where filled markers represent the in-plane thermal conductivity [9,24] and open markers represent the cross-plane thermal conductivity [6,7,16–20]. As shown in Fig. 2, the model calculation using $n_v = 2.7 \times 10^{18}$ cm^{-3} best describes the in-plane thermal conductivity data. We thus use this vacancy concentration, yielding $k_{GaN} = 119$ W m^{-1} K^{-1} at room temperature.

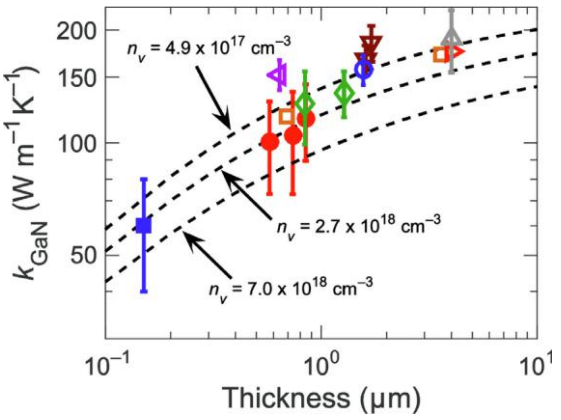

Fig. 2. Literature data for thermal conductivity of GaN films as a function of film thickness at room temperature. Filled markers represent in-plane thermal conductivity [9,24], while open markers represent cross-plane thermal conductivity [6,7,16–20]. Black dashed lines represent the predictions of the in-plane thermal conductivity model with varying vacancy concentration levels n_v.

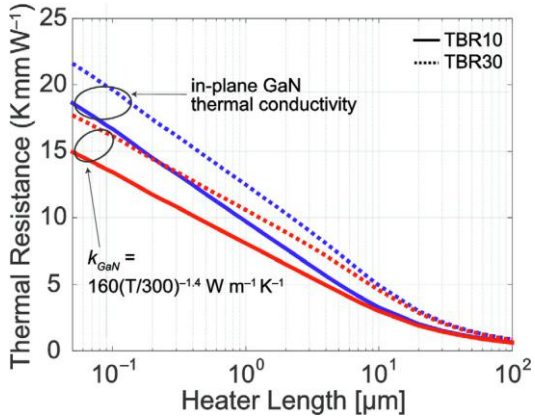

Fig. 3. GaN-on-diamond device thermal resistance versus heater length at 5 W mm^{-1}. Blue lines correspond to when we use the temperature-dependent in-plane GaN thermal conductivity, calculated assuming a vacancy defect concentration of 2.7×10^{18} cm^{-3}, while red lines correspond to when we use $k_{GaN} = 160(T/300)^{-1.4}$ W m^{-1} K^{-1}, as typically assumed as the GaN epilayer thermal conductivity in most previous thermal simulations. Solid and dashed lines represent the GaN/diamond TBRs of 10 and 30 m^2 K GW^{-1}, respectively.

3. Results and discussion

We first consider GaN-on-diamond with a single heater whose length is varied from 0.05 to 100 μm. As a first approximation, the heater length here effectively represents the characteristic lateral dimension of a heat generation region in GaN transistors [1,12]. We note that the issue of heat generation in an RF device is a complex function of device geometry, bias conditions, etc. [12]. In our present work, it is approximated as a rectangular surface heat generation to consider a generic case, as previously done by many prior publications on GaN transistors [1,2,12,13,21–23].

Fig. 3 shows the device thermal resistance of the GaN-on-diamond structure as a function of heater length at a fixed power dissipation P of 5 W mm^{-1} with using 10 and 30 m^2 K GW^{-1} as the GaN/diamond TBR and assuming inhomogeneous/anisotropic diamond. Two cases are compared: one is when we use the temperature-dependent in-plane GaN thermal conductivity, calculated assuming $n_v = 2.7 \times 10^{18}$ cm^{-3}, while the other is when we use $k_{GaN} = 160(T/300)^{-1.4}$ W m^{-1} K^{-1}, as typically assumed in most previous thermal simulations for GaN device structures [21–23]. In general, the latter underpredicts the thermal resistance of GaN-on-diamond devices when compared to the former, especially when the heater length is less than or comparable to 1 μm. This highlights the importance of the lateral spreading resistance within the GaN layer, as well as the TBR, at this dimension of the heater. The use of the in-plane thermal conductivity of the GaN epilayer is therefore essential for an accurate thermal simulation of GaN-on-diamond devices, especially given that a heat generation region in a single-gate GaN transistor is highly localized near the gate region of the device with an ~0.4 μm lateral dimension [12]. Most previous simulations for GaN-on-diamond devices do not use the in-plane GaN thermal conductivity and thereby they may underpredict the GaN-on-diamond thermal resistance.

As the heater length becomes very large (e.g., approaching 100 μm), the two cases become almost equivalent, because at this heater length, the impact of the GaN spreading resistance and the TBR becomes almost irrelevant, and the one-dimensional conduction resistance of the substrate dominates [1]. Note that, however, the heater length above 1 μm is not relevant for GaN transistors unless they are in a fully open channel condition [12,21,22]. The actual heat regeneration region in multi-finger GaN transistors consists of several, distributed single-gate heat generation regions.

As a next step we consider a multi-finger transistor cell geometry (12 fingers and 30 μm gate-to-gate spacing (s)) and evaluate the thermal performance of the state-of-the-art GaN-on-diamond and GaN-on-SiC structures that are discussed in Section 2. We assume a 0.4 μm-long power dissipation region at the gate edge on the drain side in each finger. Fig. 4(a) shows lateral temperature rise profiles of both structures at the upper GaN surfaces at $P = 5$ W mm^{-1}; see black and green solid lines. (Note: For the GaN-on-diamond, black and red solid lines correspond to when we assume inhomogeneous/anisotropic diamond, whereas a blue solid line corresponds to when we assume anisotropic but homogeneous diamond). The maximum temperature rises, which occur near the central fingers in each device, are ~106 and ~65 K, which translate to thermal resistances of ~21.2 and ~13.0 K mm W^{-1}., for the GaN-on-SiC and GaN-on-diamond devices, respectively. This demonstrates that the GaN-on-diamond thermally outperforms the GaN-on-SiC.

Fig. 4(b) shows the maximum temperature rise versus power dissipation P for the GaN-on-diamond and GaN-on-SiC devices. The difference in the maximum temperature rise between the two devices is greater at higher power dissipations. For example, as compared by black and green solid lines, the maximum temperature rise of the GaN-on-SiC is approximately 1.7X and 2.1X larger than that of the GaN-on-diamond at $P = 5$ and 12 W mm^{-1}, respectively. For the GaN-on-diamond, 10 and 20 μm gate-to-gate spacings, which correspond to black dotted and dashed lines, respectively, are also considered to examine the influence of this parameter on the device thermal resistance. With

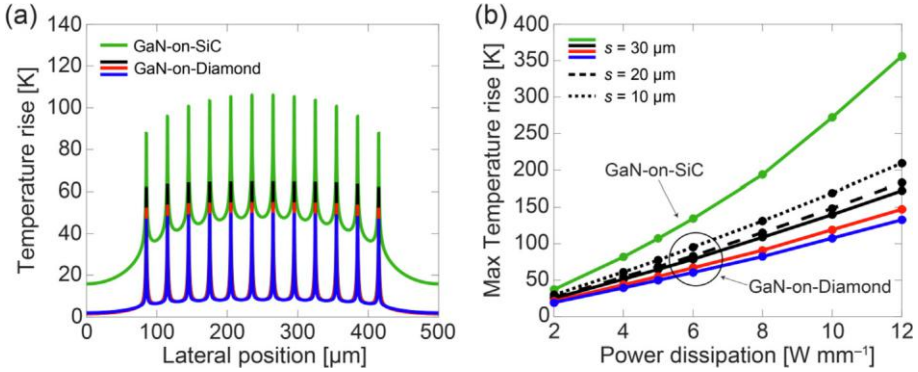

Fig. 4. (a) Lateral temperature rise profiles of multifinger GaN-on-diamond and GaN-on-SiC devices (12 fingers and 30 μm gate-to-gate spacing (s)) at the upper GaN surfaces at $P = 5$ W mm^{-1}. (b) Maximum temperature rise versus power dissipation. Solid lines correspond to $s = 30$ μm, while dotted and dashed lines correspond to $s = 10$ and 20 μm, respectively. (a and b) The green and black solid lines represent the state-of-the-art GaN-on-SiC and GaN-on-diamond devices, respectively. The red solid line represents the GaN-on-diamond device in the absence of phonon scattering by external defects in the GaN layer and interface. For the black and red solid lines, we assume inhomogeneous/anisotropic diamond. The blue solid line represents when we assume anisotropic but homogeneous diamond, as well as the absence of defect scattering in the GaN layer and interface.

decreasing gate-to-gate spacing, the maximum device temperature rise tends to increase as the heat flux generated in each finger may affect each other. The impact of the gate-to-gate spacing is more pronounced at higher power dissipation; for instance, the difference in the maximum temperature rise between 10 and 30 μm gate-to-gate spacings is ~19% at $P = 5\,\mathrm{W\,mm^{-1}}$ and ~22% at $P = 12\,\mathrm{W\,mm^{-1}}$ (compare black dotted and solid lines).

We then assess the phonon conduction limits for the current GaN-on-diamond device structure. The thermal resistance in GaN device structures is determined primarily by the strength of phonon scattering due to defects and interfaces. The minimum (maximum) possible thermal resistance (conductance) for the current GaN-on-diamond device structure can be therefore achieved in the absence of phonon scattering by external defects in the GaN layer and interface. To estimate the maximum possible thermal conductivity of the 1 μm GaN layer in the GaN-on-diamond thermal model, we use the in-plane thermal conductivity model, as described earlier, but do not consider phonon scattering by external defects. We do consider phonon scattering on isotopes, and the isotope scattering strength of 2.74×10^{-4} [27]—which can be translated to a minimum defect concentration of $4.9 \times 10^{17}\,\mathrm{cm^{-3}}$ in the GaN layer; see the topmost black dashed line in Fig. 2—yields $k_{GaN} = 140\,\mathrm{W\,m^{-1}\,K^{-1}}$ at room temperature. Previous diffuse mismatch model calculations have predicted the TBR at the direct contact interface between GaN and diamond to be $\sim 3\,\mathrm{m^2\,K\,GW^{-1}}$ [1,9]. We take this value as the lower limit of the GaN-diamond TBR. With considering these and assuming inhomogeneous/anisotropic diamond, the GaN-on-diamond device thermal resistance that may be achieved in the absence of defect scattering is predicted to be $\sim 11.0\,\mathrm{K\,mm\ W^{-1}}$ for the 12 finger device with 30 μm gate-to-gate spacing at $P = 5\,\mathrm{W\,mm^{-1}}$, which is ~49% lower than the state-of-the-art GaN-on-SiC device thermal resistance at the same dissipated power and gate-to-gate spacing; compare red and green sold lines in Fig. 4.

We further note that the assumption of anisotropic but homogeneous diamond further lowers the GaN-on-diamond thermal resistance. In this case, we use the temperature-dependent cross-plane and in-plane thermal conductivities averaged over the entire diamond thickness, as discussed earlier. Using these for the diamond, together with assuming the absence of phonon scattering by external defects, the lowest possible thermal resistance of GaN-on-diamond devices is estimated to be $\sim 10.0\,\mathrm{K\,mm\,W^{-1}}$ for the 12 finger device with 30 μm gate-to-gate spacing at $P = 5\,\mathrm{W\,mm^{-1}}$, which is ~54% lower than the GaN-on-SiC thermal resistance at the same dissipated power and gate-to-gate spacing; compare blue and green sold lines in Fig. 4.

4. Conclusions

This work investigates the fundamental limits to near-junction conduction cooling of GaN-on-diamond devices by evaluating their lowest possible device thermal resistance. The device thermal resistance of a state-of-the-art GaN-on-diamond structure is predicted to be $13.0\,\mathrm{K\,mm\ W^{-1}}$ for a 12 finger device with 30 μm gate-to-gate spacing and a power dissipation of $5\,\mathrm{W\,mm^{-1}}$, which is ~39% lower than that of a state-of-the-art GaN-on-SiC structure for the same multifinger cell geometry and dissipated power. In the absence of phonon scattering by external defects in the GaN layer and interface, the GaN-on-diamond device thermal resistance is predicted to be $\sim 11.0\,\mathrm{K\,mm\ W^{-1}}$ for the same multifinger cell geometry and dissipated power. With assuming anisotropic but homogeneous diamond, as well as the absence of defect scattering, the lowest possible thermal resistance of GaN-on-diamond devices is estimated to be $\sim 10.0\,\mathrm{K\,mm\ W^{-1}}$ for the same multifinger cell geometry and dissipated power, which is ~54% lower than the GaN-on-SiC thermal resistance.

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References

[1] J. Cho, Z. Li, M. Asheghi, K.E. Goodson, Annu. Rev. Heat Transf. 18 (2014) 1.
[2] Y. Won, J. Cho, D. Agonafer, M. Asheghi, K.E. Goodson, IEEE Trans. Compon. Packag. Manuf. Technol. 5 (2015) 737.
[3] A. Bar-Cohen, J.J. Maurer, A. Sivananthan, MRS Adv. 1 (2016) 181.
[4] J.A. del Alamo, J. Joh, Microelectron. Reliab. 49 (2009) 1200.
[5] D.C. Dumka, T.M. Chou, F. Faili, D. Francis, F. Ejeckam, Electron. Lett. 49 (2013) 1298.
[6] J. Cho, Y. Li, W.E. Hoke, D.H. Altman, M. Asheghi, K.E. Goodson, Phys. Rev. B 89 (2014) 115301.
[7] J. Cho, E. Bozorg-Grayeli, D.H. Altman, M. Asheghi, K.E. Goodson, IEEE Electron. Device Lett. 33 (2012) 378.
[8] L. Yates, J. Anderson, X. Gu, C. Lee, T. Bai, M. Mecklenburg, T. Aoki, M.S. Goorsky, M. Kuball, E.L. Piner, S. Graham, ACS Appl. Mater. Interfaces 10 (2018) 24302.
[9] J. Cho, D. Francis, D.H. Altman, M. Asheghi, K.E. Goodson, J. Appl. Phys. 121 (2017) 055105.
[10] H. Sun, R.B. Simon, J.W. Pomeroy, D. Francis, F. Faili, D.J. Twitchen, M. Kuball, Appl. Phys. Lett. 106 (2015) 111906.
[11] Y. Zhou, J. Anaya, J. Pomeroy, H. Sun, X. Gu, A. Xie, E. Beam, M. Becker, T.A. Grotjohn, C. Lee, M. Kuball, ACS Appl. Mater. Interfaces 9 (2017) 34416.
[12] S. Rajasingam, J.W. Pomeroy, M. Kuball, M.J. Uren, T. Martin, D.C. Herbert, K.P. Hilton, R.S. Balmer, IEEE Electron. Device Lett. 25 (2004) 456.
[13] J. Anaya, H. Sun, J. Pomeroy, M. Kuball (Eds.), Proceedings of the IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, 2016 Las Vegas, USA.
[14] A. Sood, J. Cho, K.D. Hobart, T.I. Feygelson, B.B. Pate, M. Asheghi, D.G. Cahill, K.E. Goodson, J. Appl. Phys. 119 (2016) 175103.
[15] J. Cho, Nanoscale Microscale Thermophys. Eng. 22 (2018) 6.
[16] V. Asnin, F.H. Pollak, J. Ramer, M. Schurman, I. Ferguson, Appl. Phys. Lett. 75 (1999) 1240.
[17] Y.K. Koh, Y. Cao, D.G. Cahill, D. Jena, Adv. Funct. Mater. 19 (2009) 610.
[18] E. Ziade, J. Yang, G. Brummer, D. Nothern, T. Moustakas, A.J. Schmidt, Appl. Phys. Lett. 107 (2015) 091605.
[19] T.L. Bougher, L. Yates, C.F. Lo, W. Johnson, S. Graham, B.A. Cola, Nanoscale Microscale Thermophys. Eng. 20 (2016) 22.
[20] T.E. Beechem, A.E. McDonald, E.J. Fuller, A.A. Talin, C.M. Rost, J.P. Maria, J.T. Gaskins, P.E. Hopkins, A.A. Allerman, J. Appl. Phys. 120 (2016) 095104.
[21] A. Sarua, H. Ji, K.P. Hilton, D.J. Wallis, M.J. Uren, T. Martin, M. Kuball, IEEE Electron. Device Lett. 54 (2007) 3152.
[22] J.W. Pomeroy, M. Bernardoni, D.C. Dumka, D.M. Fanning, M. Kuball, Appl. Phys. Lett. 104 (2014) 083513.
[23] K. Park, C. Bayram, Appl. Phys. Lett. 109 (2016) 151904.
[24] C. Hodges, J.A. Calvo, S. Stoffels, D. Marcon, M. Kuball, Appl. Phys. Lett. 103 (2013) 202108.
[25] A. Jeżowski, B.A. Danilchenko, M. Bockowski, I. Grzegory, S. Krukowski, T. Suski, T. Paszkiewicz, Solid State Commun. 128 (2003) 69.
[26] C. Dames, G. Chen, J. Appl. Phys. 95 (2004) 682.
[27] D.T. Morelli, J.P. Heremans, G.A. Slack, Phys. Rev. B 66 (2002) 195304.