

Thermal Design and Fabrication of Embedded Liquid Cooling for Gallium Nitride High Electron Mobility Transistor Devices

Received 29 November, 2024; accepted 4 December, 2024

Minsoo Kang^{a,b,†}, Hyun-Wook Jung^{b,†}, Junrae Park^{a,b}, Ilgyu Choi^b, Sung-Jae Chang^b, Seong-Il Kim^b, Jong-Won Lim^b, Ho-Kyun Ahn^{b,*}, and Hyoungsoon Lee^{a,c,*}

^aDepartment of Intelligent Energy and Industry, Chung-Ang University, Seoul 06974, Republic of Korea

^bRF/Power Components Research Section, Electronics and Telecommunications Research Institute, Daejeon 34129, Republic of Korea

^cSchool of Mechanical Engineering, Chung-Ang University, Seoul 06974, Republic of Korea

[†]These authors contributed equally to this work.

*Corresponding author E-mail: hkahn@etri.re.kr, leeh@cau.ac.kr

ABSTRACT

The thermal design and fabrication of a manifold microchannel structure for liquid cooling embedded in gallium nitride high electron mobility transistor radio frequency devices were investigated. Three microchannel designs with widths of 50, 100, and 200 μm were assessed, and computational analysis was performed to evaluate their thermal performance and optimize the silicon carbide (SiC) substrate thickness. Consequently, the feasibility of the embedded microchannel structure was validated through an inductively coupled plasma-etching-based fabrication on a SiC substrate. The results showed that at maximum pumping power (P_{pump}), a smaller channel width exhibited better thermal performance, with a temperature difference of 28.3 $^{\circ}\text{C}$. Subsequently, thickness optimization was conducted for the configuration with the best thermal performance structure of microchannel width (50 μm) and fin width (50 μm). The results indicated that at a low P_{pump} , a thicker channel tended to exhibit better thermal performance. However, at high P_{pump} , where thermal performance was improved, the optimal point was attained at a thinner structure with a thickness of 75 μm . Furthermore, optimization of the etching process successfully eliminated micropillars formed when a large amount of SiC was etched, resulting in a smooth pillar-free microchannel structure.

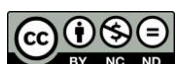
Keywords: AlGaIn/GaN, High electron mobility transistor, Embedded cooling, Thermal modeling, Fabrication

1. Introduction

Advancements in wireless communication technologies and the development of long-range detection radar systems have significantly expanded the radio frequency (RF) market. Among the critical components driving this growth, high-power amplifiers (HPAs) play a vital role in enabling long-range transmission. Gallium nitride (GaN) has emerged as a highly suitable material for RF HPAs owing to its exceptional material properties, including high breakdown field, high carrier concentration, and excellent electron mobility. These characteristics make GaN-based devices ideal for satisfying the stringent demands of high-power RF applications [1–3]. Consequently, substantial research has been devoted to the development and optimization of GaN-based power amplifiers [4–8]. Their ability to operate efficiently at high frequencies and high-power levels is promising for modern RF system designs. However, the high-power operation of these devices inevitably causes significant thermal challenges [9,10]. The dissipation of excess heat generated during operation limits its optimal performance and reliability [11]. Consequently, improving the thermal management of GaN-based power amplifiers has become an area of interest in both academic and industrial research.

Traditional cooling methods for RF devices often rely on indirect approaches, such as cold plates or forced air cooling to manage thermal loads [12–14]. Building on Tuckerman and Pease's pioneering work on microchannels, researchers have explored direct cooling strategies to minimize the conduction thermal resistance by embedding microchannels directly into device substrates [15–19]. Recent studies focused on manifold microchannel designs to achieve uniform heat dissipation and reduce pressure drops by optimizing fluid flow paths [20–22]. However, these high-performance thermal management structures have been applied to automotive power converters and data-center computing systems, with limited adaptation to RF devices. The compact size of the RF power amplifiers necessitates new design principles for implementing direct cooling systems. Additionally, the distinct geometry of the heat-generating areas in RF power amplifiers, compared with other power semiconductors, requires thermal management solutions tailored to their unique characteristics.

In this study, computational simulations were conducted to evaluate thermal performance improvements in manifold microchannels specifically designed for RF power amplifiers. An RF GaN high electron mobility transistor (HEMT) power amplifier was used as a model to analyze the thermal and hydraulic performances across the three embedded microchannel designs with various channel configurations.



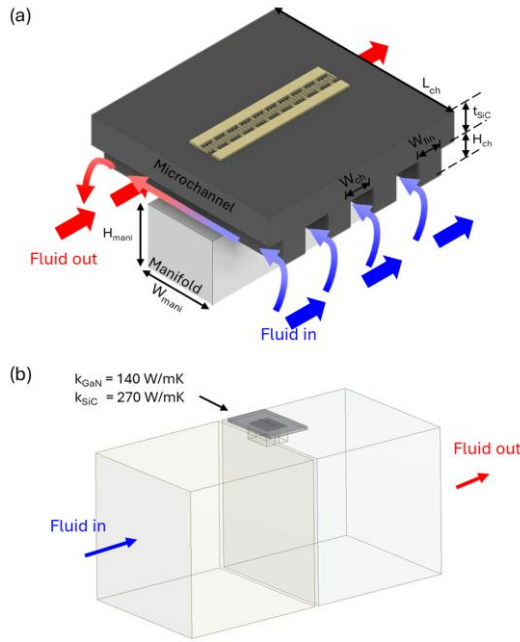


Figure 1. (a) The detailed device structure used for computational fluid dynamics simulation. (b) Overall view of the computational fluid dynamics structure and material properties.

In addition, a GaN HEMT power amplifier with an integrated microchannel structure is fabricated to assess the practical manufacturability and performance of different channel configurations, providing valuable insights into the feasibility of implementing such designs in RF devices.

2. Method

2.1. Thermal hydraulic modeling

Computational fluid dynamics simulations were performed using ANSYS Fluent v19.2. Figure 1 shows a schematic of the simulation setup. The RF GaN HEMT power amplifier was modeled with a total gate width of 4.8 mm, comprising 40 gates, each with a unit gate width of $120 \mu\text{m}$, based on a single transistor bar. Heat generation was assumed to occur in the depletion region between the gate and source, with a gate length of $0.5 \mu\text{m}$, as referenced in [23,24]. The die size was set to $4.5 \text{ mm} \times 3.0 \text{ mm}$ to account for the bonding area required for practical fabrication. Two analyses were conducted to optimize the thermal performance: one examined the effect of channel width (W_{ch}) variations on the thermal performance, and the other focused on optimizing the performance with respect to the silicon carbide (SiC) substrate thickness (t_{SiC}). The channel width was varied from 50 to $200 \mu\text{m}$, while all other parameters were held constant. The t_{SiC} was initially set to $100 \mu\text{m}$ and the thermal performance of various channel designs was compared. Based on the $W_{ch} = 100 \mu\text{m}$ channel structure, substrate thickness optimization was performed. The detailed geometrical parameters are summarized in the Table I. Here, the fin width (W_{fin}), the microchannel height (H_{ch}), and the microchannel length (L_{ch}) are represented. Additionally, the GaN thickness (t_{GaN}), the manifold width of the package (W_{mani}), and the manifold height (H_{mani}) are also represented.

Table I. Geometrical parameters of the manifold microchannel structure in μm .

W_{ch}	W_{fin}	H_{ch}	L_{ch}	t_{SiC}	t_{GaN}	W_{mani}	H_{mani}
50, 100, 200	50	100	1,000	50 – 150	1.8	300	1,000

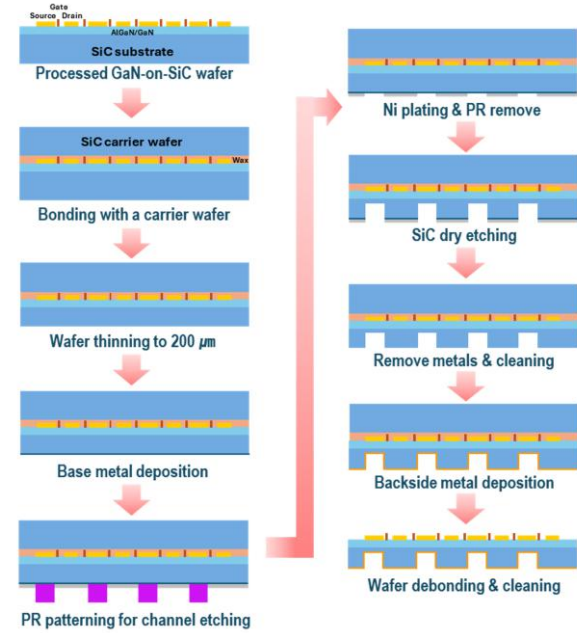


Figure 2. Etching process of SiC microchannel.

A mass-flow inlet boundary condition was applied to the inlet, defined by a volumetric flow rate (Q) ranging from 10 to 50 ml/min , and the pressure P outlet was set to 0 kPa . A constant heat flux (q'') of 25.6 kW/cm^2 was applied to the active area ($1.56 \text{ mm} \times 0.12 \text{ mm}$). The turbulence model was selected based on prior studies, with the $k-\epsilon$ model and enhanced wall treatment employed, as it is well-suited for manifold microchannel structures [25,26].

The analysis results were evaluated based on the maximum chip temperature and pumping power, with the pumping power (P_{pump}) calculated as the product of the volumetric flow rate and pressure difference.

$$P_{\text{pump}} = Q \times \Delta P \quad (1)$$

2.2. Fabrication of embedded channel on SiC substrate

Based on a computational study, a GaN HEMT device with an embedded microchannel structure was fabricated. The fabrication process is illustrated in Fig. 2. First, the device was mounted on a carrier wafer using wax to ensure protection, and the SiC substrate was ground to a thickness of $200 \mu\text{m}$. Thereafter, the residual particles were cleaned sequentially with acetone, isopropyl alcohol, and deionized (DI) water, followed by additional cleaning via ashing and DI water cleaning. For electroplating, a base metal layer of Ti/Au ($3/8 \text{ nm}$) was deposited via e-beam evaporation. The microchannel was patterned using photolithography, followed by nickel electroplating. The photoresist was removed in the following sequence: Acetone, isopropyl alcohol, DI water, ashing, and DI water. The SiC was etched using inductively coupled plasma dry etching with sulfur hexafluoride (SF_6) gas. The etch steps were varied as follows: $100 \mu\text{m}$ (1 step), $10 \mu\text{m}$ (10 steps), and $5 \mu\text{m}$ (20 steps). After etching, Ni was removed using a nitric acid:DI water solution (1:2 ratio), Au was removed using an Au etchant, and Ti was removed using a buffer oxide etchant:DI water solution (6:1 ratio). Finally, the etching residues were removed through ultrasonic cleaning in a hydrochloric acid:DI water solution (1:2 ratio), and the carrier wafer was detached using a hot plate.

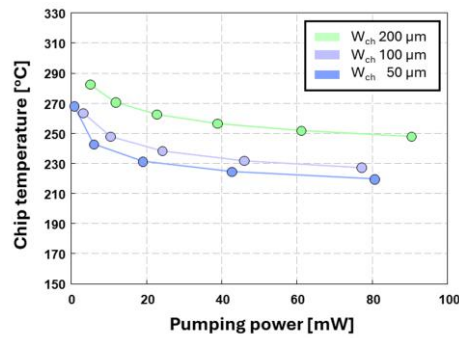


Figure 3. Thermal performance analysis results based on W_{ch} variation.

3. Results and discussion

3.1. Result of thermal performance with various flowrate

Figure 3 shows the results of the thermal performance analysis of the manifold microchannel-embedded RF device based on W_{ch} and P_{pump} . Using this manifold microchannel cooling structure, the operating temperature could be maintained below 225 °C under high-heat-generation conditions. At lower P_{pump} levels, the thermal performance improved significantly; however, as P_{pump} increased to higher levels, the improvement in thermal performance became negligible, despite a substantial increase in the flowrate. For the same P_{pump} , smaller W_{ch} values indicated better performance. This is because a smaller channel width increases the heat exchange surface area, thereby improving efficiency. Moreover, a smaller channel width causes an increase in flow velocity, which enhances the impingement effect on the heat-generated region. At a P_{pump} of 80 – 90 mW, where thermal performance has saturated, the device shows a temperature difference of 28.3 °C between W_{ch} of 50 and 200 μm.

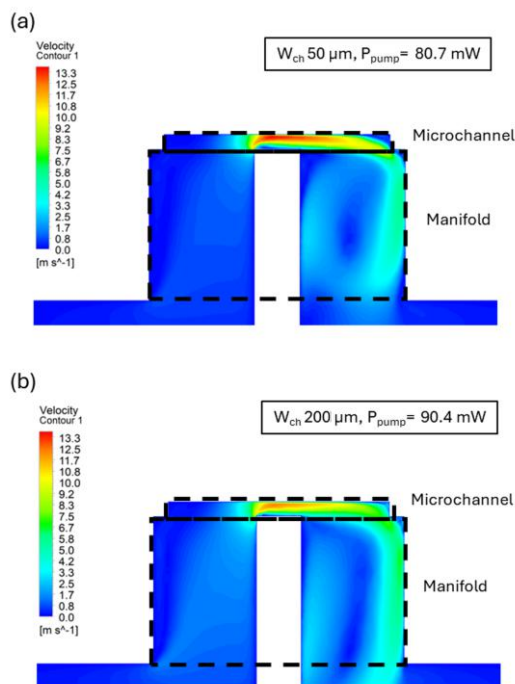


Figure 4. Hot spot impingement effect based on channel width. Fluid velocity contour of (a) $W_{ch} = 50 \mu\text{m}$ and (b) $W_{ch} = 200 \mu\text{m}$.

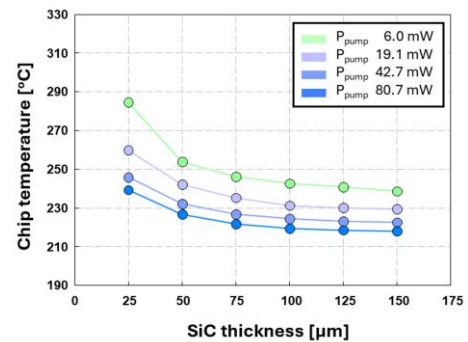


Figure 5. Analysis of optimal substrate thickness based on thermal performance.

Figure 4 shows the fluid velocity contour for the case with $W_{ch} = 50$ and $200 \mu\text{m}$ at P_{pump} of 80.7 – 90.4 mW. The contour indicates that the fluid directly impinges below the heat-generating region of the RF power amplifier, which features a narrow and elongated heat-dissipation area that enhances thermal performance. At the maximum velocity in the microchannel, where impingement was induced by the manifold wall increased from 12.4 to 13.8 m/s, the device temperature dropped from 247.7 to 219.4 °C, owing to increased P_{pump} contributes to the variation in thermal performance.

Figure 5 shows the thermal performance optimization results for a microchannel with $W_{ch} = 50 \mu\text{m}$ and $W_{fin} = 50 \mu\text{m}$ as a function of the SiC substrate thickness. The analysis was conducted with substrate thicknesses ranging from 25 to 150 μm, and the P_{pump} was varied from 6.0 to 80.7 mW. For a lower P_{pump} , which corresponds to a lower thermal performance, optimal thermal performance was achieved with a thicker substrate. However, for higher P_{pump} , which corresponds to

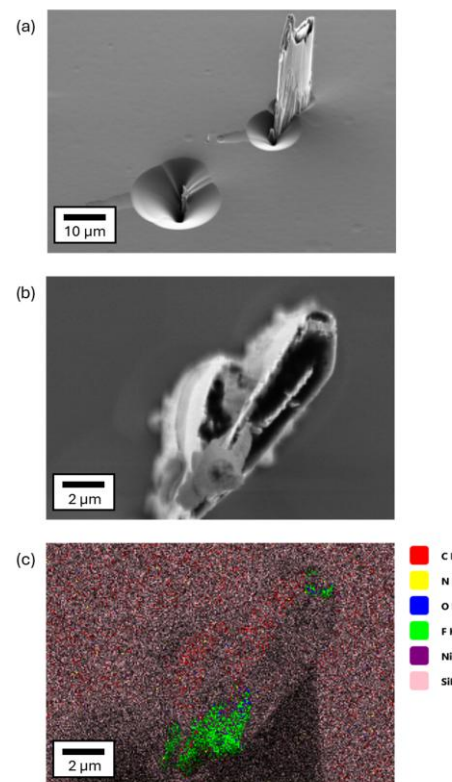


Figure 6. (a) SEM image of micropipe and micro pillar. (b) SEM image for EDS analysis and (c) EDS result.

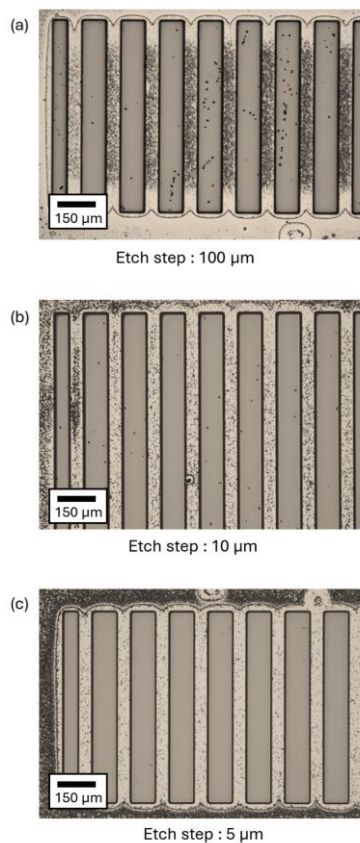


Figure 7. Microchannel optical image of (a) etch step = 100 μm , (b) 10 μm , and (c) 5 μm .

better thermal performance, optimal performance was observed with a thinner substrate ($t_{\text{SiC}} = 100 \mu\text{m}$). The temperature reduction owing to an increase in t_{SiC} had a significant impact at a low P_{pump} of 0.8 mW. At P_{pump} levels above 6 mW, when t_{SiC} exceeds 100 μm , the temperature difference was observed to be less than 1 $^{\circ}\text{C}$.

3.2. Fabrication of embedded microchannel GaN HEMT transistor

Figure 6 shows the micropillars formed during fabrication. Figure 6(a) shows that the etching by-products accumulated in the micropipes, forming micropillars. During the etching process, the SF_6 gas used for etching becomes concentrated in the micropipes, causing the temperature to increase further in these regions. This causes an increase in the etching rate. Excessive byproducts generated at higher etch rates accumulate in the micropipes, forming structures resembling micropillars. The detailed mechanism of micropillar formation is explained in the study by Okamoto *et al.* [27]. Figure 6(b) displays a scanning electron microscope (SEM) image of micropillar and Fig. 6(c) shows the results of energy-dispersive X-ray spectroscopy (EDS) analysis performed to identify the composition of the micropillars. The EDS analysis revealed that the micropillars were composed of Si, C, and F, indicating that they were impurities formed by the reaction of SiC and F during the etching of SiC, which is consistent with the findings of Okamoto's research. The number of etching steps was increased to suppress the formation of micropillars. Between steps, the Descum process was conducted to clean the excessively generated byproducts, and sufficient time was allowed for the device to cool.

Figure 7(a) presents optical microscopy images of the GaN HEMT device depending on the etching step. The sample was fabricated un-

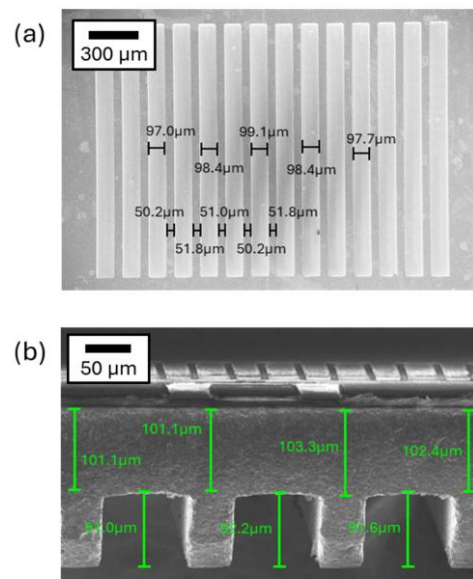


Figure 8. (a) Measurement of channel width and fin width using top-view SEM image. (b) Measurement of SiC substrate height and channel height using side-view SEM image.

der the original etching conditions, resulting in the formation of micropillars. Figure 7(b) shows an image etched in steps of 10 μm , while Fig. 7(c) shows an image etched in steps of 5 μm . By increasing the etching step and frequently performing the descending process, the formation of micropillars was effectively suppressed. Figure 8 shows the SEM images of the final GaN-on-SiC HEMT device with a microchannel structure. In particular, Fig. 8(a) shows that the fabricated microchannel achieved a W_{ch} of 97 – 99 μm and a W_{fin} of 50 – 52 μm , while Fig. 8(b) confirms an H_{ch} of 91 – 92 μm and a t_{SiC} of 101 – 103 μm . These results demonstrate that the microchannels were fabricated with the desired dimensions, ensuring effective integration of the microchannel structure into the GaN HEMT device.

4. Conclusions

In this study, a thermal performance analysis and manufacturability validation were conducted to develop a manifold microchannel structure on a GaN-on-SiC device. Thermal-hydraulic optimization focuses on variations in the channel width and substrate thickness. The analysis revealed that smaller W_{ch} values enhanced the thermal performance of the same P_{pump} owing to the increased heat exchange area between the fluid and device. Manufacturability was evaluated for the embedded manifold microchannel structures in GaN HEMT RF amplifiers. During fabrication, larger etching steps were found to cause etching byproducts to accumulate in the micropipes, resulting in micropillar formation. Pillar-free microchannels were successfully fabricated by optimizing etching steps. The fabricated device confirmed that the design parameters derived from the analysis were implemented accurately, validating the proposed design and fabrication methodology.

Acknowledgments

This study was supported by the Civil Military Technology Cooperation Program (Grant No. 19-CM-BD-05).

Conflicts of Interest

The authors declare no conflicts of interest.

ORCID

Minsoo Kang <https://orcid.org/0000-0003-4719-3076>
 Hyun-Wook Jung <https://orcid.org/0000-0001-5770-6387>
 Junrae Park <https://orcid.org/0009-0001-4301-466x>
 Ilgyu Choi <https://orcid.org/0000-0002-5566-3050>
 Ho-Kyun Ahn <https://orcid.org/0000-0003-3937-8257>
 Hyounghoon Lee <https://orcid.org/0000-0001-5961-6393>

References

- [1] U. K. Mishra, L. Shen, T. E. Kazior, and Y. F. Wu, *Proc. IEEE* 96, 287 (2008).
- [2] Y. Cao *et al.*, *IEEE/MTT-S International Microwave Symposium* (Los Angeles, USA, August 4-6, 2020), p. 520.
- [3] R. J. Liu *et al.*, *IEEE Trans. Microw. Theory Tech.* 70, 3910 (2022).
- [4] L. S. McCarthy *et al.*, *IEEE Trans. Electron Dev.* 48, 543 (2001).
- [5] D. Guerra, M. Saraniti, D. K. Ferry, S. M. Goodnick, and F. A. Marino, *IEEE Trans. Electron Dev.* 58, 3876 (2011).
- [6] A. P. Zhang, F. Ren, T. J. Anderson, C. R. Abernathy, R. K. Singh, P. H. Holloway, S. J. Pearton, D. Palmer, and G. E. McGuire, *Crit. Rev. Solid State Mater. Sci.* 27, 1 (2002).
- [7] I. Choi, S. J. Chang, D. Kim, J. W. Lim, D. M. Kang, H. W. Jung, and H. K. Ahn, *Appl. Sci. Conver. Technol.* 33, 144 (2024).
- [8] D. Kim, H. W. Jung, S. J. Chang, I. G. Choi, H. K. Ahn, and H. S. Lee, *Appl. Sci. Conver. Technol.* 33, 152 (2024).
- [9] Y. Won, J. Cho, D. Agonafer, M. Asheghi, and K. E. Goodson, *IEEE Trans. Comp. Packag. Manuf. Technol.* 5, 737 (2015).
- [10] A. Bar-Cohen, J. J. Maurer, and D. H. Altman, *J. Electron. Packag.* 141, 040803 (2019).
- [11] F. Temcamani, J. B. Fonder, O. Latry, and C. Duperrier, *IEEE Trans. Microw. Theory Tech.* 64, 756 (2016).
- [12] G. Zhang, J. W. Pomeroy, M. E. Navarro, H. Cao, M. Kuball, and Y. Ding, *IEEE Trans. Comp. Packag. Manuf. Technol.* 11, 748 (2021).
- [13] W. Hong, L. Zhang, C. Zhang, F. Zhang, S. Z. Yue, P. B. Du, X. F. Zheng, X. H. Ma, and Y. Hao, *Appl. Phys. Lett.* 124, 182203 (2024).
- [14] A. Baba, O. Silva, B. Sugumaran, W. Khattak, A. Alebri, M. AlMansoori, F. Vega, and C. Kasmi, *Proceedings of the 23rd IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems* (Aurora, USA, May 28-31, 2024), pp. 1-7.
- [15] D. B. Tuckerman and R. F. W. Pease, *IEEE Electron Dev. Lett.* 2, 126 (1981).
- [16] D. Kong *et al.*, *Int. J. Heat Mass Transfer* 141, 145 (2019).
- [17] H. Liu, Y. Yao, G. Xie, and Z. Xie, *Appl. Therm. Eng.* 196, 117293 (2021).
- [18] H. Zhou, J. Lee, M. Kang, H. Kim, H. Lee, and J. B. In, *Mater. Des.* 221, 110968 (2022).
- [19] D. Jung *et al.*, *Int. J. Heat Mass Transf.* 175, 121192 (2021).
- [20] R. van Erp, R. Soleimanzadeh, L. Nela, G. Kampitsis, and E. Mattioli, *Nature* 585, 211 (2020).
- [21] H. Kwon *et al.*, *Int. Commun. Heat Mass Transfer* 156, 107592 (2024).
- [22] D. Kong, H. Kwon, B. Jang, H. J. Kwon, M. Asheghi, K. E. Goodson, and H. Lee, *Energy Convers. Manag.* 315, 118809 (2024).
- [23] M. P. Gupta, A. K. Vallabhaneni, and S. Kumar, *IEEE Trans. Comp. Packag. Manuf. Technol.* 7, 1305 (2017).
- [24] H. Zhang, Z. Guo, and Y. Lu, *IEEE Trans. Electron Dev.* 67, 47 (2020).
- [25] A. Elkholy, O. Khaled, and R. Kempers, *20th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems* (San Diego, USA, June 1-4, 2021), p. 9.
- [26] H. C. Cui, W. H. Fan, J. Wang, M. J. Yu, Z. K. Zhang, Z. C. Liu, and W. Liu, *Appl. Therm. Eng.* 245, 122769 (2024).
- [27] N. Okamoto, *J. Vac. Sci. Technol. A* 27, 295 (2009).